DWG ISSUE	CD ISSUE	DWG ISSUE	CD ISSUE	DWG ISSUE	CD ISSUE
1	1				

DWG ISSUE	CD ISSUE	DATE ISSUED	[illegible]	APP'D
2A	1 APPX 1A	11-10-75	AS DNR	JEJ LEG RFG
3B	1 APPX 2B	5-7-76	DNR	JEJ LEG RFG
4D	1 APPX 3D	7-19-77	[illegible] TCH	CE LEG JBD
5AC	2AC	7-19-77	NATAL TCH	CE LEG JBD

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
SHEET INDEX SUPPORTING INFORMATION USED ON	A1	1	2	3	4	5																				
APPARATUS INDEX	A2	1	2	2	4	5																				
FS 1 SERIAL PERIPHERAL INTERFACE	B1AA		2	2	2	5																				
	B1AR		2	2	2	5																				
	B1CA	1	2	2	2	5																				
	B1CB					5																				
FS 2 BUS TERMINATOR	B2AA		2	2	2	5																				
	B2AB		2	2	2	5																				
	B2CA	1	2	2	2	5																				
FS 3 BUFFER	B3AA		2	2	2	5																				
	B3AB		2	2	2	5																				
	B3CA	1	2	2	2	5																				
	B3GA		2	2	2	2																				
	B3GB		2	2	2	2																				
	B3GC		2	2	2	2																				
	B3GD		2	2	2	2																				
	B3GE		2	2	2	2																				
	B3GF		2	2	2	2																				
	B3GG		2	2	2	2																				
	B3GH		2	2	2	2																				
	B3GJ		2	2	2	2																				
	B3GK		2	2	2	2																				
FS 4 CARTRIDGE TAPE TRANSPORT CONTROLLER	B4AA		2	2	2	5																				
	B4AB		2	2	2	5																				
	B4CA	1	2	2	2	5																				
	B4CB	1	2	2	2	5																				
	B4GA		2	2	2	2																				
	B4GB		2	2	2	2																				
	B4GC		2	2	2	2																				
	B4GD		2	2	2	2																				
	B4GE		2	2	2	2																				
	B4GF		2	2	2	5																				
FS 5 CARTRIDGE TAPE TRANSPORT	B5AA		2	2	2	2																				
	B5AB		2	2	2	5																				
	B5CA	1	2	2	2	5																				
FS 6 POWER	B6AA		2	2	4	5																				
	B6AB		2	2	2	5																				
	B6CA	1	2	2	4	5																				
SHEET CANCELED ON DWG ISS 5AC	B6CB																									
FS 7 SYNCHRONOUS DATA SET CONTROLLER	B7AA					5																				
	B7AB					5																				
	B7CA					5																				
	B7GA					5																				
	B7GB					5																				
	B7GC					5																				
	B7GD					5																				
APP FIG. 1	C1	1	2	2	4	5																				

CONTENTS	SHEET NO.	ISSUE NO.																								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
CIRCUIT NOTES EQUIPMENT NOTES INFORMATION NOTES	D1	1	2	2	4	5																				
CAD NOTES	GB1	1	2	3	2	5																				
CAD 1 UNIT SYMBOL	GB2	1	2	2	2	5																				
CADS 2-9	GB3	1	2	2	2	2																				
CAD 10-15, P/O CAD 16	GB4	1	2	2	2	2																				
P/O CAD 16, CAD 17,18,19	GB5	1	2	2	2	5																				

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING, ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK SCHEMATIC	CPS-X
EQUIPMENT DRAWING	J1C053A
KS-21447 MINIRECORDER CKT	SD-97736-01
DC-DC CONVERTER (J87421A)	SD-82327-01

X - SCHEMATICS OF ALL FA,FB,FC AND JK-CODED CIRCUIT PACKS USED IN THIS CIRCUIT ARE SHOWN ON DRWINGS NUMBERED WITH A CPS PREFIX FOLLOWED BY THE CODE OF THE PACK, e.g., CPS-JK10

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE 5AC

1N98

COMMON SYSTEMS

TAPE DATA CONTROLLER
CIRCUIT

②

AT&TCO
STANDARD

SD-1C904-01-A1
52 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

APPARATUS INDEX

EQUIP LOC	APP NO.	FIGURE SH NO.
CIRCUIT PACKS		
05-16	1	C1
05-17	1	C1
05-19	1	C1
05-20	1	C1
05-21	1	C1
05-22	1	C1
05-24	2	C1
05-25	2	C1
05-27	1	C1
05-28	1	C1
05-29	1	C1
05-31	1	C1
05-32	1	C1
05-33	1	C1
05-34	1	C1
DESIG		
BT-A	1	C1
BT-R	1	C1
BUF-A	1	C1
BUF-B	1	C1
BUF-C	1	C1
BUF-D	1	C1
CTTC-A	1	C1
CTTC-B	1	C1
CTTC-C	1	C1
CTTC-D	1	C1
SDSC-A	2	C1
SDSC-B	2	C1
SP1-A	1	C1
SP1-B	1	C1
SPI-C	1	C1

DESIG	LOCATION FS/SYM	LOCATION APPFIG	LOCATION EQPT
CIRCUIT PACK-CP			
BT-A	2/1	1	05-17
BT-B	2/2	1	05-16
BUF-A	3/1	1	05-31
BUF-B	3/2	1	05-29
BUF-C	3/3	1	05-28
BUF-D	3/4	1	05-27
CTTC-A	4/1	1	05-22
CTTC-B	4/2	1	05-21
CTTC-C	4/3	1	05-20
CTTC-D	4/4	1	05-19
SDSC-A	7/1	2	05-25
SDSC-B	7/2	2	05-24
SP1-A	1/1	1	05-34
SP1-B	1/2	1	05-33
SPI-C	1/3	1	05-32
CT TRANSPORT			
CTT-J5	5/2	1	04-10R
CTT-J6	5/1	1	04-04R
POWER MODULE			
PM1	6/1	1	05-39
PM2	6/2	1	05-44
SWITCH			
SW1	6/3	1	01-39

ISSUE
5AC

TAPE DATA CONTROLLER

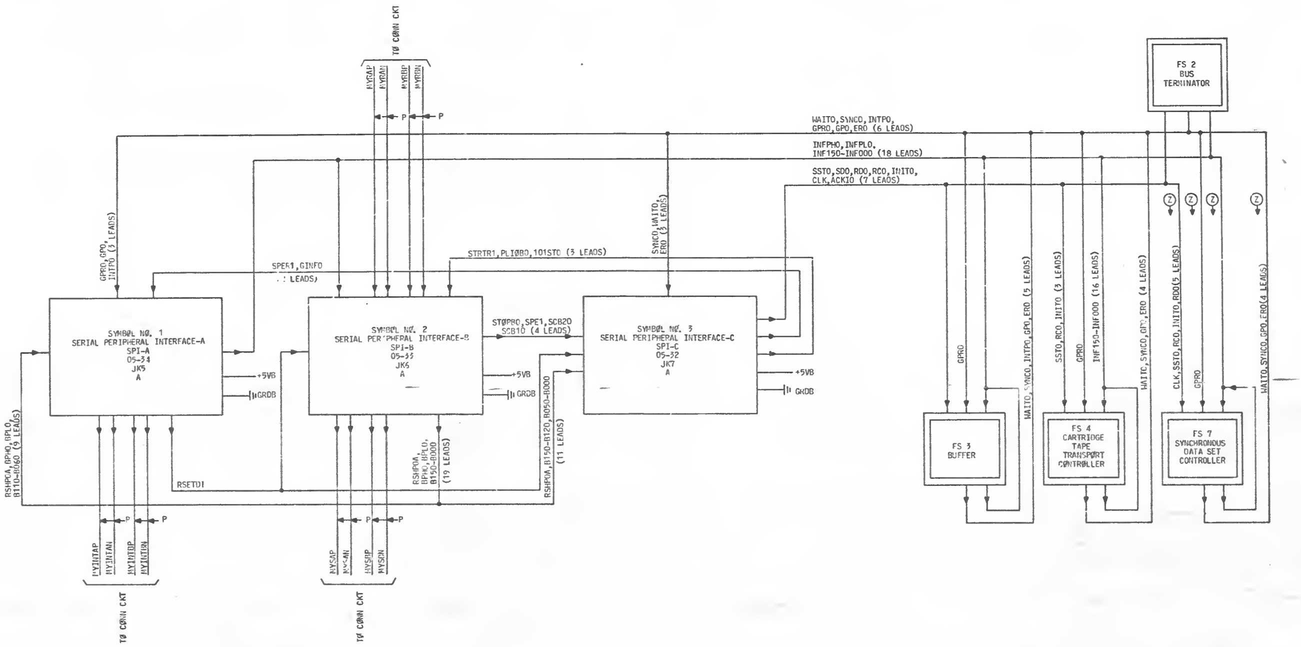
BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C904-01-A2

PART OF FS I

SERIAL PERIPHERAL INTERFACE
INTERCONNECTION AND FLOW DIAGRAM



PART OF FS 1
INTERCONNECTION AND FLOW DIAGRAM

TAPE DATA CONTROLLER ②

DWG SIZE 65
ISSUE 5AC

BELL LABORATORIES
SD-1C904-01
BIAA

PART OF FS 1

SERIAL PERIPHERAL INTERFACE

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+5VB	+5 VOLT POWER BUS B
ACKI0	ACKNOWLEDGE INTERRUPT COMMAND, ACTIVE LOW
BPH0	BUFFERED PARITY HIGH BIT
BPL0	BUFFERED PARITY LOW BIT.
B(00-15)0	BUFFERED BUS BITS 00 THROUGH 15
CLK	COMMON PARALLEL BUS SQUARE WAVE CLOCK PULSE TRAIN WITH 600 NS PERIOD
ER0	REQUEST TO THE SPI TO TRANSMIT AN ERROR START CODE IN THE CURRENT STATUS REPLY TO THE CC, LOW ACTIVE
GINF0	GATE ONTO INFORMATION BUS
GPR0	REPLY FROM BT TO ACKNOWLEDGE THE RECEIPT OF A GP0 REQUEST, ACTIVE LOW
GP0	REQUEST TO BT TO GENERATE PARITY OVER THE STATUS REPLY CURRENTLY RESIDING ON THE COMMON PARALLEL BUS
GROB	GROUND RETURN FOR +5V POWER BUS B
INFPH0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 HIGH-ORDER DATA BITS, LOW = LOGICAL ONE
INFPL0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 LOW-ORDER DATA BITS, LOW = LOGICAL ONE
INF(00-15)0	COMMON PARALLEL BUS BITS (00-15), LOW = LOGICAL ONE
INIT0	TDC INITIALIZE COMMAND, LOW ACTIVE
INTP0	CC-INTERRUPT FOR OFF-LINE BUFFER SERVICING, ACTIVE LOW
MYINTAN	MY INTERRUPT A OUTPUT NEGATIVE LEAD TO ASSOCIATED CC
MYINTAP	MY INTERRUPT A OUTPUT POSITIVE LEAD TO ASSOCIATED CC
MYINTBN	MY INTERRUPT B OUTPUT NEGATIVE LEAD TO OTHER CC
MYINTBP	MY INTERRUPT B OUTPUT POSITIVE LEAD TO OTHER CC
MYRAN	MY RECEIVE A INPUT NEGATIVE LEAD FROM ASSOCIATED CC
MYRAP	MY RECEIVE A INPUT POSITIVE LEAD FROM ASSOCIATED CC
MYRBN	MY RECEIVE B INPUT NEGATIVE LEAD FROM OTHER CC
MYRBP	MY RECEIVE B INPUT POSITIVE LEAD FROM OTHER CC
MYSAN	MY SEND A OUTPUT NEGATIVE LEAD TO ASSOCIATED CC
MYSAP	MY SEND A OUTPUT POSITIVE LEAD TO ASSOCIATED CC
MYSBN	MY SEND B OUTPUT NEGATIVE LEAD TO OTHER CC
MYSBP	MY SEND B OUTPUT POSITIVE LEAD TO OTHER CC
PLIOB0	PARALLEL LOAD IOB REGISTER
RC0	ADDRESS DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS AND INTERPRET THEM AS A COMMAND, LOW ACTIVE

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
RD0	ADDRESS DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS, ACTIVE LOW
RSETD1	RESET THE SPI
RSHP0A	RECOVERED SHIFT PULSE
SCB10	START CODE BIT 1
SCB20	START CODE BIT 2
SD0	ADDRESSED DEVICE TO SEND DATA TO THE SPI ON THE COMMON PARALLEL BUS, ACTIVE LOW
SPER1	SERIAL PARITY ERROR REPLY
SPE1	SERIAL PARITY ERROR
SST0	ADDRESSED DEVICE REQUESTED TO GATE A STATUS REPLY ON THE COMMON PARALLEL BUS, ACTIVE LOW
STOPB0	STOP BUFFERED SIGNAL
STRTR1	START REPLY
SYNC0	A SYNCHRONIZING SIGNAL TO THE SPI WHICH INDICATES THAT A DEVICE HAS SENSED A COMMAND ON THE PARALLEL BUS, ACTIVE LOW
WAIT0	A REQUEST TO THE SPI TO WAIT UNTIL THE DEVICE HAS HAD TIME TO ACT UPON A COMMAND BEFORE REMOVING THAT COMMAND FROM THE COMMON PARALLEL BUS, ACTIVE LOW
101ST0	101 START CODE

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

B1AB

PRINTED IN U. S. A.

06/15/77

PART OF FS 1

SERIAL PERIPHERAL INTERFACE

SYMBOL NO. 1

SERIAL PERIPHERAL INTERFACE - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPI-A	05-34	JK5	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
		001			BSD1	3G2
		019			PTORO	3G1
+5VB	PWR	000		203	+5V	
	PWR	119		203	+5V	
BPHO	I	104	1/2		BPHO	2A0
BPLO	I	108	1/2		BPLO	2A4
B000	I	004	1/2		B000	2A9
B010	I	0G9	1/2		B010	2A8
B020	I	105	1/2		B020	2A7
B030	I	007	1/2		B030	2A6
B040	I	309	1/2		B040	2A6
B050	I	300	1/2		B050	2A5
B060	I	107	1/2		B060	2A5
B070	I	008	1/2		B070	2A5
B080	I	014	1/2		B080	2A3
B090	I	005	1/2		B090	2A3
B100	I	201	1/2		B100	2A2
B110	I	308	1/2		B110	2A2
B120	I	003	1/2		B120	2A1
B130	I	103	1/2		B130	2A1
B140	I	102	1/2		B140	2A1
B150	I	002	1/2		B150	2A0
GINFO	I	106	1/3		GINFO	2A4
GPRO	I	101	2/1		GPRO	3A5
GPO	I	202	3/1		GPO	3A6
GRDB	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INFPHO	OT	203	2/2,3/3		INFPHO	2G0
	I		1/2			
INFPLO	OT	301	2/2,3/3		INFPLO	2G4
	I		1/2			
INF000	OT	215	2/2,3/1		INF000	2G9
			3/3,4/1			
	I		1/2,3/1			
			(2)7/1			
INF010	OT	314	2/2,3/1		INF010	2G8
			3/3			
	I		1/2,3/1			
			4/1,(2)7/1			
INF020	O	211	2/2,3/3		INF020	2G7
			4/1			
			1/2,3/1			
			(2)7/1			
INF030	OT	310	2/2,3/1		INF030	2G6
			3/3,4/1			
	I		1/2,3/1			
			(2)7/1			
INF040	O	116	2/2,3/3		INF040	2G6
			1/2,3/1			
			4/1,(2)7/1			
INF050	O	214	2/2,3/3		INF050	2G5
			1/2,3/1			
			4/1,(2)7/1			
INF060	OT	205	2/2,3/1		INF060	2G9
			3/3,4/4			
			(2)7/2			
	I		1/2			
INF070	OT	304	2/2,3/1		INF070	2G5
			3/3,4/4			
			(2)7/2			
	I		1/2,4/1			
INF080	OT	206	2/2,3/1		INF080	2G3
			3/3,4/1			
			4/4,(2)7/2			
	I		1/2			
INF090	OT	305	2/2,3/1		INF090	2G3

SYMBOL NO. 1 (CONT)

SERIAL PERIPHERAL INTERFACE - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPI-A	05-34	JK5	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
			3/3,4/1			
			4/4,(2)7/2			
	I		1/2,3/1			
			(2)7/1			
INF100	OT	010	2/2,3/1		INF100	2G2
			3/3,4/1			
			4/4,(2)7/2			
	I		1/2,3/1			
			(2)7/1			
INF110	OT	109	2/2,3/1		INF110	2G2
			3/3,4/1			
			4/4			
	I		1/2,3/1			
			(2)7/1			
INF120	OT	207	2/2,3/1		INF120	2G1
			3/3,4/1			
			4/4			
	I		1/2,3/1			
			(2)7/1			
INF130	OT	307	2/2 3/1		INF130	2G1
			3/3,4/1			
			4/4			
	I		1/2,3/1			
			(2)7/1			
INF140	OT	312	2/2,3/1		INF140	2G1
			3/3,4/1			
			4/4			
	I		1/2,3/1			
			(2)7/1			
INF150	OT	212	2/2,3/1		INF150	2G0
			3/3,4/1			
			4/4,(2)7/1			
	I		1/2,3/1			
INTPO	I	302	2/1		INTPO	3A4
MYINTAN	O	219	TO CONN CKT	P/MYINTAP 202	MYINTAN	3G5
MYINTAP	O	318	TO CONN CKT	P/MYINTAN 202	MYINTAP	3G4
MYINTBN	O	218	TO CONN CKT	P/MYINTBP 202	MYINTBN	3G5
MYINTBP	O	317	TO CONN CKT	P/MYINTBN 202	MYINTBP	3G5
RSETD1	O	217	1/2,1/3		RSETD1	3G2
RSHPOA	I	100	1/2		RSHPOA	3A1
SPER1	I	006	1/3		SPER1	2A9

SYMBOL NO. 2

SERIAL PERIPHERAL INTERFACE - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPI-B	05-33	JK6	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
		201			3VI	3D9
+5VB	PWR	000		203	+5V	
	PWR	119		203	+5V	
BPHO	O	102	1/1		BPHO	2G0
BPLO	O	107	1/1		BPLO	2G4
B000	O	113	1/1,1/3		B000	2G7
B010	O	014	1/1,1/3		B010	2G7
B020	O	100	1/1,1/3		B020	2G6
B030	O	117	1/1,1/3		B030	2G6
B040	O	016	1/1,1/3		B040	2G5
B050	O	101	1/1,1/3		B050	2G5
B060	O	001	1/1		B060	2G4
B070	O	104	1/1		B070	2G4
B080	O	008	1/1		B080	2G3
B090	O	313	1/1		B090	2G3
B100	O	114	1/1		B100	2G2
B110	O	103	1/1		B110	2G2
B120	O	004	1/1,1/3		B120	2G2
B130	O	019	1/1,1/3		B130	2G1
B140	O	018	1/1,1/3		B140	2G1
B150	O	002	1/1,1/3		B150	2G0
GRDB	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INFPHO	I	203	1/1		INFPHO	2A0
INFPLO	I	206	1/1		INFPLO	2A3
INF000	I	215	1/1		INF000	2A7
INF010	I	314	1/1		INF010	2A7
INF020	I	211	1/1		INF020	2A6
INF030	I	310	1/1		INF030	2A6
INF040	I	116	1/1		INF040	2A5
INF050	I	214	1/1		INF050	2A5
INF060	I	205	1/1		INF060	2A4
INF070	I	304	1/1		INF070	2A4
INF080	I	301	1/1		INF080	2A4
INF090	I	003	1/1		INF090	2A3
INF100	I	010	1/1		INF100	2A2
INF110	I	109	1/1		INF110	2A2
INF120	I	207	1/1		INF120	2A2
INF130	I	307	1/1		INF130	2A1
INF140	I	312	1/1		INF140	2A1
INF150	I	212	1/1		INF150	2A0
MYRAN	I	311	TO CONN CKT	P/MYRAP 202	MYRAN	3A0
MYRAP	I	213	TO CONN CKT	P/MYRAN 202	MYRAP	3A0
MYRBN	I	208	TO CONN CKT	P/MYRBP 202	MYRBN	3A1
MYRBP	I	308	TO CONN CKT	P/MYRBN 202	MYRBP	3A0
MYSAN	O	118	TO CONN CKT	P/MYSAP 202	MYSAN	3H0
MYSAP	O	218	TO CONN CKT	P/MYSAN 202	MYSAP	3H0
MYSBN	O	219	TO CONN CKT	P/MYSBP 202	MYSBN	3H1
MYSBP	O	318	TO CONN CKT	P/MYSBN 202	MYSBP	3H1
PLIOBO	I	317	1/3		PLIOBO	2A0
RSETD1	I	006	1/1		RSETD1	3A5
RSHPOA	O	105	1/1,1/3		RSHPOA	2G6

SYMBOL NO. 2 (CONT)

SERIAL PERIPHERAL INTERFACE - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPI-B	05-33	JK6	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		FS INFO			CP INFO	
SCB10	O	017	1/3		SCB010	2G7
SCB20	O	115	1/3		SCB020	2G7
SPE1	O	315	1/3		SPE1	3H7
STOPBO	O	005	1/3		STOPBO	2G8
STRTR1	I	217	1/3		STRTR1	3A7
101STO	I	309	1/3		101STO	2A7

PART OF FS 1
SYMBOL(S) 1 2

TAPE DATA CONTROLLER

DWG SIZE C2
ISSUE 5AC

BELL LABORATORIES
SD-1C904-01
B1CA

PRINTED IN U. S. A.
07/13/77

PART OF FS 1
SERIAL PERIPHERAL INTERFACE

SYMBOL NO. 3
SERIAL PERIPHERAL INTERFACE - C

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SPI-C	05-32	JK7	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
+5VB	PWR	000		203	+5V	
	PWR	119		203	+5V	
ACK10	0	003	2/1,3/1		ACK10	2H1
B000	1	202	1/2		B000	2A3
B010	1	201	1/2		B010	2A3
B020	1	300	1/2		B020	2A2
B030	1	002	1/2		B030	2A4
B040	1	101	1/2		B040	2A3
B050	1	100	1/2		B050	2A3
B120	1	301	1/2		B120	2A1
B130	1	302	1/2		B130	2A1
B140	1	001	1/2		B140	2A1
B150	1	203	1/2		B150	2A0
CLK	0	103	2/1,3/1 (2)7/1		CLK	2H6
ER0	1	117	2/1		ER0	3A7
GINFO	0	013	1/1		GINFO	3H3
GRDB	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INIT0	0	318	2/1,3/1 4/1,(2)7/1		INIT0	2H1
PLIOB0	0	112	1/2		PLIOB0	3H2
RC0	0	216	2/1,3/1 4/1,(2)7/1		RC0	2H4
RD0	0	007	2/1,3/1 (2)7/1		RD0	2H5
RSETD1	1	014	1/1		RSET1	3A8
	1	113	1/1		RSETD1	3A5
RSHP0A	1	111	1/2		RSHP0A	2A5
SCB10	1	010	1/2		SCB10	2A5
SCB20	1	102	1/2		SCB20	2A4
SD0	0	011	2/1,3/1		SD0	2H0
SPER1	0	114	1/1		SPER1	2H9
SPE1	1	018	1/2		SPE1	2A7
SST0	0	217	2/1,3/1 4/4,(2)7/1		SST0	2H1
STOPB0	1	118	1/2		STOPB0	2A8
STRTR1	0	110	1/2		STRTR1	3H6
SYNC0	IO	303	2/1		SYNC0	2A5
WAIT0	1	104	2/1		WAIT0	2A7
101ST0	0	019	1/2		101ST0	2H8

PART OF FS 1
SYMBOL(S) 3

TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
B1CB
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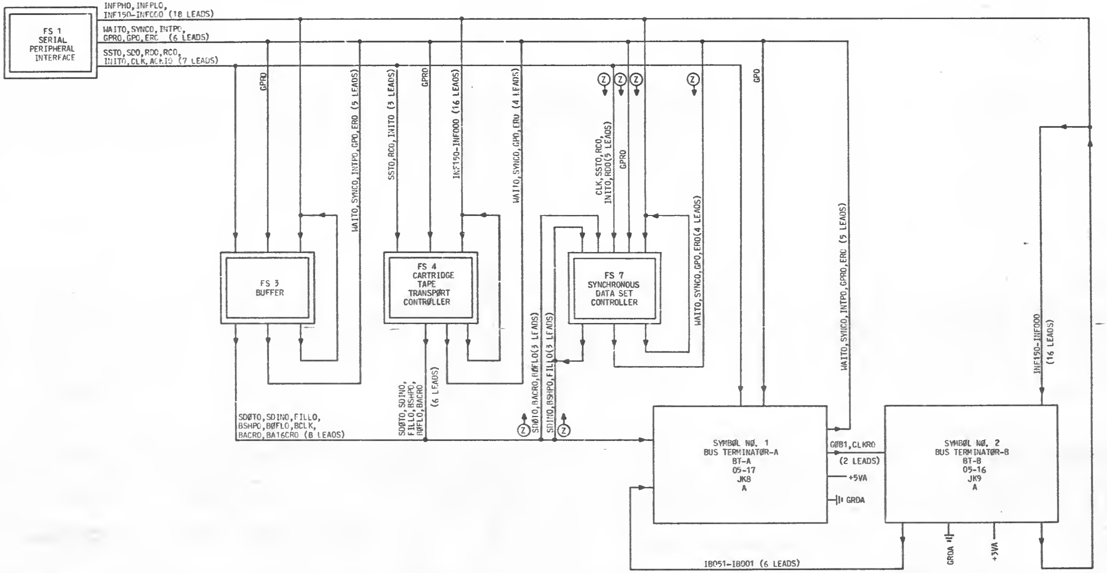
07/13/77

PART OF FS 2

BUS TERMINATOR
INTERCONNECTION AND FLOW DIAGRAM


FS 1 SERIAL PERIPHERAL INTERFACE
INFPHO, INFPLO, INF150-INF000 (18 LEADS)
WAITO, SYNCO, INTPO, GPRO, GPO, ERC (6 LEADS)
SSTO, SDO, RDO, RCO, INITO, CLK, ACKIO (7 LEADS)
GPRO
WAITO, SYNCO, INTPO, GPO, ERO (5 LEADS)
SSTO, RCO, INITO (3 LEADS)
GPRO
INF150-INF000 (16 LEADS)
WAITO, SYNCO, GPO, ERO (4 LEADS)
CLK, SSTO, RCO, INITO, RDO (5 LEADS)
GPRO
Z
Z
Z
Z
GPO
FS 3 BUFFER
FS 4 CARTRIDGE TAPE TRANSPORT CONTROLLER
FS 7 SYNCHRONOUS DATA SET CONTROLLER
WAITO, SYNCO, GPO, ERO (4 LEADS)
WAITO, SYNCO, INTPO, GPRO, ERC (5 LEADS)
INF150-INF000 (16 LEADS)
SDOTO, SDINO, FILLO, BSHPO, BOFLO, BCLK, BACRO, BA16CRO (8 LEADS)
SDOTO, SDINO, FILLO, BSHPO, BOFLO, BACRO
(6 LEADS)
SDOTO, BACRO, BOFLO (3 LEADS)
SDINO, BSHPO, FILLO (3 LEADS)
Z
Z
SYMBOL NO. 1 BUS TERMINATOR-A BT-A 05-17 JK8 A
GOB1, CLKRO
(2 LEADS)
+5VA
GRDA
SYMBOL NO. 2 BUS TERMINATOR-B BT-B 05-16 JK9 A
IB051-IB001 (6 LEADS)
GRDA
+5VA

PART OF FS 2
INTERCONNECTION AND FLOW DIAGRAM

TAPE DATA CONTROLLER 2

DWG SIZE
6S

ISSUE
SAC

BELL LABORATORIES

SD-1C904-01

B2AA

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PART OF FS 2

BUS TERMINATOR

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+5VA	+5 VOLT POWER BUS A
ACKI0	ACKNOWLEDGE INTERRUPT COMMAND, ACTIVE LOW
BACR0	SERIAL BUFFER BUS CARRY PULSE INDICATING THAT THE ON-LINE (ACTIVE) DATA BUFFER HAS BEEN EITHER FILLED OR EMPTIED, ACTIVE LOW
BA16CR0	SERIAL BUFFER BUS 16 BIT CARRY PULSE INDICATING THAT A 16-BIT WORD HAS BEEN TRANSFERRED BETWEEN THE ON LINE DATA BUFFER AND THE DEVICE CONNECTED TO IT, ACTIVE LOW
BCLK	SERIAL BUFFER BUS CLOCK-SQUARE WAVE PULSE TRAIN WITH 600 NS PERIOD
BOFL0	SERIAL BUFFER BUS OVERFLOW INDICATION, ACTIVE LOW
BSHP0	SERIAL BUFFER BUS DATA SHIFT PULSE, ACTIVE LOW
CLK	COMMON PARALLEL BUS SQUARE WAVE CLOCK PULSE TRAIN WITH 600 NS PERIOD
CLKR0	CLOCK HOLDING REGISTER
ER0	REQUEST TO THE SPI TO TRANSMIT AN ERROR START CODE IN THE CURRENT STATUS REPLY TO THE CC, ACTIVE LOW
FILL0	SERIAL BUFFER BUS FILL OPERATION REQUEST, ACTIVE LOW
GDB1	GATE ONTO BUS
GPR0	REPLY FROM BT TO ACKNOWLEDGE THE RECEIPT OF A GP0 REQUEST, LOW ACTIVE
GP0	REQUEST TO BT TO GENERATE PARITY OVER STATUS REPLY CURRENTLY RESIDING ON THE COMMON PARALLEL BUS
GRDA	GROUND RETURN FOR +5V POWER BUS A
IBD(0-5)1	INTERNAL BUFFERED BUS LEADS BITS 00 THROUGH 05
INFPH0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 HIGH-ORDER DATA BITS, LOW = LOGICAL ONE
INFPL0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 LOW-ORDER DATA BITS, LOW = LOGICAL ONE
INF(00-15)0	COMMON PARALLEL BUS BITS (00-15), LOW = LOGICAL ONE
INIT0	TDC INITIALIZE COMMAND, LOW ACTIVE
INTP0	CC-INTERRUPT FOR OFF-LINE BUFFER SERVICING, ACTIVE LOW
RC0	ADDRESS DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS AND INTERPRET THEM AS A COMMAND, LOW ACTIVE
RD0	ADDRESSED DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS, ACTIVE LOW
SDIN0	SERIAL BUFFER BUS DATA INPUT TO THE BUFFER UNIT, LOW = LOGICAL ONE
SDOT0	SERIAL BUFFER BUS DATA OUTPUT FROM THE BUFFER UNIT, LOW = LOGICAL ONE
SD0	ADDRESSED DEVICE TO SEND DATA TO THE SPI ON COMMON PARALLEL BUS, ACTIVE LOW
SST0	ADDRESSED DEVICE REQUESTED TO GATE A STATUS REPLY ON THE COMMON PARALLEL BUS, ACTIVE LOW
SYNC0	A SYNCHRONIZING SIGNAL TO THE SPI WHICH INDICATES THAT A DEVICE HAS SENSED A COMMAND ON THE PARALLEL BUS, ACTIVE LOW
WAIT0	A REQUEST TO THE SPI TO WAIT UNTIL THE DEVICE HAS HAD TIME TO ACT UPON A COMMAND BEFORE REMOVING THAT COMMAND FROM THE COMMON PARALLEL BUS, ACTIVE LOW

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES SD-1C904-01

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PART OF FS 2

BUS TERMINATOR

SYMBOL NO. 1

BUS TERMINATOR - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BT-A	05-17	JK8	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		118			BSPARE	2A6
		201			INHBR0	2A8
		301			STUFF0	2A8
		317			RDY0	2H1
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
ACKI0	I	115	1/3		ACKI0	2A4
BACR0	I	300	3/4		BACR0	2A7
BA16CR0	I	213	3/4		BA16CR0	2A8
BCLK	I	314	3/2		BCLK	2A9
BOFL0	I	313	3/2		BOFL0	2A7
BSHP0	I	019	4/3		BSHP0	2A6
CLK	I	103	1/3		CLK	2A6
CLKR0	O	003	2/2		CLKR0	2H3
ER0	OT	117	3/1,4/4 (2)7/1		ER0	2H0
	I		1/3			
FILL0	I	316	4/3		FILL0	2A9
GOB1	O	004	2/2		GOB1	2H8
GPR0	O	101	1/1,3/1 4/4,(2)7/1		GPR0	2H6
GP0	I	202	3/1		GP0	2A5
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
IB001	I	110	2/2		IB001	2A1
IB011	I	109	2/2		IB011	2A1
IB021	I	009	2/2		IB021	2A0
IB031	I	010	2/2		IB031	2A0
IB041	I	011	2/2		IB041	2A0
IB051	I	111	2/2		IB051	2A0
INIT0	I	116	1/3		INIT0	2A4
INTP0	OT	302	3/1		INTP0	2H1
	I		1/1			
RC0	I	216	1/3		RC0	2A2
RD0	I	007	1/3		RD0	2A2
SDIN0	I	218	3/2		SDIN0	2A7
SDOT0	I	018	3/4		SDOT0	2A7
SD0	I	016	1/3		SD0	2A3
SST0	I	217	1/3		SST0	2A3
SYNC0	OT	303	3/1,4/4 (2)7/1		SYNC0	2H3
	I		1/3			
WAIT0	OT	104	3/1,4/4 (2)7/1		WAIT0	2H7
	I		1/3			

SYMBOL NO. 2

BUS TERMINATOR - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BT-B	05-16	JK9	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
CLKR0	I	009	2/1		CLKR0	2A2
GOB1	I	102	2/1		GOB1	2A1
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
IB001	O	117	2/1		IB001	2C9
IB011	O	017	2/1		IB011	2C9
IB021	O	018	2/1		IB021	2C9
IB031	O	118	2/1		IB031	2C9
IB041	O	013	2/1		IB041	2C9
IB051	O	113	2/1		IB051	2C9
INFPH0	OT	203	1/1		INFPH0	2H2
INFPL0	OT	301	1/1		INFPL0	2H6
INF000	OI	215	1/1		INF000	2H9
INF010	OI	314	1/1		INF010	2H8
INF020	OI	211	1/1		INF020	2H8
INF030	OI	310	1/1		INF030	2H8
INF040	OI	116	1/1		INF040	2H7
INF050	OI	214	1/1		INF050	2H7
INF060	OI	205	1/1		INF060	2H7
INF070	OI	304	1/1		INF070	2H6
INF080	OI	206	1/1		INF080	2H6
INF090	OI	305	1/1		INF090	2H4
INF100	OI	010	1/1		INF100	2H4
INF110	OI	109	1/1		INF110	2H3
INF120	OI	207	1/1		INF120	2H3
INF130	OI	307	1/1		INF130	2H3
INF140	OI	312	1/1		INF140	2H2
INF150	OI	212	1/1		INF150	2H2

PART OF FS 2
SYMBOL(S) 1 2

TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
B2CA
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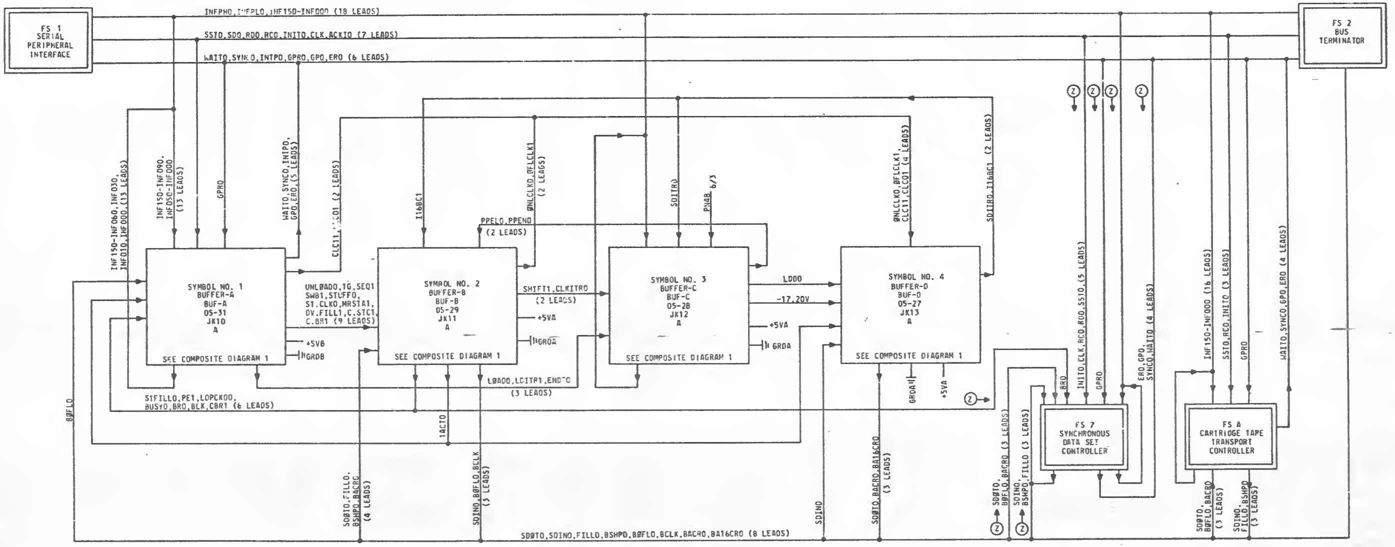
07/13/77

PART OF FS 3

BUFFER
INTERCONNECTION AND FLOW DIAGRAM



PART OF FS 3
INTERCONNECTION AND FLOW DIAGRAM

TAPE DATA CONTROLLER

	DWG SIZE	ISSUE
	6S	5AC
BELL LABORATORIES	SD-1C904-01	B3AA

PART OF FS 3

BUFFER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+5VA	+5 VOLT POWER BUS A
+5VB	+5 VOLT POWER BUS B
-17.20V	INPUT TO BUFFER VOLTAGE REGULATOR
ACKI0	ACKNOWLEDGE INTERRUPT COMMAND, ACTIVE LOW
BACR0	SERIAL BUFFER BUS CARRY PULSE INDICATING THAT THE ON-LINE (ACTIVE) DATA BUFFER HAS BEEN EITHER FILLED OR EMPTIED, ACTIVE LOW
BA16CR0	SERIAL BUFFER BUS 16 BIT CARRY PULSE INDICATING THAT A 16-BIT WORD HAS BEEN TRANSFERRED BETWEEN THE ON-LINE DATA BUFFER AND THE DEVICE CONNECTED TO IT, ACTIVE LOW
BCLK	SERIAL BUFFER BUS CLOCK - SQUARE WAVE PULSE TRAIN WITH 600 NS PERIOD
BLK.CBR1	INHIBIT THE CLEARING OF THE BUFFER READY FLAG
BOFL0	SERIAL BUFFER BUS OVERFLOW INDICATION, ACTIVE LOW
BR0	OFF-LINE BUFFER READY FOR SERVICING FLAG, ACTIVE LOW
BSHP0	SERIAL BUFFER BUS DATA SHIFT PULSE, ACTIVE LOW
BUSY0	BUFFER BUSY - OFF-LINE BUFFER SEQUENCE IN PROGRESS, ACTIVE LOW
C.BR1	DECODED CLEAR BUFFER READY FLAG COMMAND, ACTIVE HIGH
C.STC1	CLEAR THE STUFF COUNTER, ACTIVE HIGH
CLC01	CLEAR THE COUNTER ASSOCIATED WITH 1024-BIT BUF0, ACTIVE HIGH
CLC11	CLEAR THE COUNTER ASSOCIATED WITH 1024-BIT BUF1, ACTIVE HIGH
CLK	COMMON PARALLEL BUS SQUARE WAVE CLOCK PULSE TRAIN WITH 600 NS PERIOD
CLKITR0	SERIALLY SHIFT THE INTERMEDIATE TRANSFER REGISTER ON THE TRAILING EDGE OF A LOW-GOING PULSE
DV.FILL1	DECODED ON-LINE BUFFER FILL MAINTENANCE COMMAND, ACTIVE LOW
ENDT0	ENABLE DATA TRANSFER - GATE THE INTERMEDIATE TRANSFER REGISTER ONTO THE COMMON PARALLEL BUS, ACTIVE LOW
ER0	REQUEST TO THE SPI TO TRANSMIT AN ERROR START CODE IN THE CURRENT STATUS REPLY TO THE CC, LOW ACTIVE
FILL0	SERIAL BUFFER BUS FILL OPERATION REQUEST, ACTIVE LOW
GPR0	REPLY FROM BT TO ACKNOWLEDGE THE RECEIPT OF A GP0 REQUEST, LOW ACTIVE
GP0	REQUEST TO BT TO GENERATE PARITY OVER THE STATUS REPLY CURRENTLY RESIDING ON THE COMMON PARALLEL BUS
GRDA	GROUND BUS A
GRDB	GROUND BUS B
INFPH0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 HIGH-ORDER DATA BITS, LOW = LOGICAL ONE

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
INFPL0	COMMON PARALLEL BUS PARITY BIT (ODD) OVER THE 8 LOW-ORDER DATA BITS, LOW = LOGICAL ONE
INF(00-15)0	COMMON PARALLEL BUS BITS (00-15), LOW = LOGICAL ONE
INIT0	TDC INITIALIZE COMMAND, LOW ACTIVE
INTP0	CC-INTERRUPT FOR OFF-LINE BUFFER SERVICING, ACTIVE LOW
I16BC1	16 BIT CARRY PULSE INDICATING THAT A 16-BIT WORD HAS BEEN TRANSFERRED BETWEEN THE OFF-LINE BUFFER AND THE INTERMEDIATE TRANSFER REGISTER, ACTIVE HIGH
LDD0	SERIAL DATA INPUT TO THE OFF-LINE BUFFER FROM THE INTERMEDIATE TRANSFER REGISTER, LOW = LOGICAL 1
LDITR1	LOAD THE INTERMEDIATE TRANSFER REGISTER FROM THE COMMON PARALLEL BUS ON A HIGH TO LOW TRANSITION
LDPCKD0	LOAD OPERATION PARITY CHECK DELAY, ACTIVE LOW. GUARANTEES THAT A PARALLEL PARITY ERROR IS REPORTED IN THE FOLLOWING STATUS REPLY
LOAD0	ENABLES THE LOADING OF THE PARALLEL PARITY BITS INTO THE INTERMEDIATE TRANSFER REGISTER FROM THE COMMON PARALLEL BUS
MRSTA1	BUFFER MASTER RESET, ACTIVE HIGH
OFLCLK1	CLOCK THE OFF-LINE BUFFER AND ITS ASSOCIATED COUNTER ON A HIGH TO LOW TRANSITION
ONLCLK0	CLOCK THE ON-LINE BUFFER AND ITS ASSOCIATED COUNTER ON A LOW TO HIGH TRANSITION
PE1	PARALLEL PARITY ERROR, ACTIVE HIGH
PN48	-48 VOLT POWER FROM TDC POWER SWITCH TO BUF CIRCUIT (SUPPLIED FROM -48VA)
PPEH0	PARALLEL PARITY ERROR IN THE HIGH ORDER BITS DURING ITR REGISTRATION, ACTIVE LOW
PPEL0	PARALLEL PARITY ERROR IN THE LOW ORDER BITS DURING ITR REGISTRATION, ACTIVE LOW
RC0	ADDRESS DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS AND INTERPRET THEM AS A COMMAND, LOW ACTIVE
RD0	ADDRESSED DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS, ACTIVE LOW
SDIN0	SERIAL BUFFER BUS DATA INPUT TO THE BUFFER UNIT, LOW = LOGICAL ONE
SDITR0	SERIAL DATA INPUT TO INTERMEDIATE TRANSFER REGISTER FROM THE OFF-LINE BUFFER, LOW = LOGICAL 1
SDOT0	SERIAL BUFFER BUS DATA OUTPUT FROM THE BUFFER UNIT, LOW = LOGICAL ONE
SD0	ADDRESSED DEVICE TO SEND DATA TO THE SPI ON THE COMMON PARALLEL BUS, ACTIVE LOW
SHIFT1	INTERMEDIATE TRANSFER REGISTER SERIAL SHIFT MODE, ACTIVE HIGH
SST0	ADDRESSED DEVICE REQUESTED TO GATE A STATUS REPLY ON THE COMMON PARALLEL BUS, ACTIVE LOW
ST.CLK0	STOP THE BUFFER CLOCK, ACTIVE LOW

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
STFILL0	FILL OPERATION IN PROGRESS STATUS INDICATION, ACTIVE LOW
STUFF0	DECODED OFF-LINE BUFFER STUFF COMMAND, ACTIVE LOW
SWB1	DECODED BUFFER SWITCH COMMAND, ACTIVE HIGH
SYNC0	A SYNCHRONIZING SIGNAL TO THE SPI WHICH INDICATES THAT A DEVICE HAS SENSED A COMMAND ON THE PARALLEL BUS, ACTIVE LOW
TG.SEQ1	TOGGLE THE FIRST ELEMENT OF THE OFF-LINE BUFFER SEQUENCER CHAIN ON A HIGH TO LOW TRANSITION
UNLOAD0	INHIBIT PARALLEL PARITY CHECKING WHILE UNLOADING THE INTERMEDIATE TRANSFER REGISTER ONTO THE COMMON PARALLEL BUS, ACTIVE LOW
WAIT0	A REQUEST TO THE SPI TO WAIT UNTIL THE DEVICE HAS HAD TIME TO ACT UPON A COMMAND BEFORE REMOVING THAT COMMAND FROM THE COMMON PARALLEL BUS, ACTIVE LOW
1ACT0	1024-BIT BUF1 IS ON-LINE (ACTIVE), ACTIVE LOW

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

B3AB

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06/15/77

PART OF FS 3

BUFFER

SYMBOL NO. 1

BUFFER - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-A	05-31	JK10	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		205			RDYO	2H0
+5VB	PWR	000		203	+5V	
	PWR	119		203	+5V	
ACKIO	I	308	1/3		ACKIO	2A7
BLK.CBR1	I	005	3/2		BLK.CBR1	3A8
BOFLO	I	207	3/2		BOFLO	3A9
BRO	I	004	3/2		BRO	2A8
BUSYO	I	302	3/2		BUSYO	2A4
C.BR1	O	105	3/2		C.BR1	3H9
C.STC1	O	111	3/2		CSTC1	3H4
CLC01	O	309	3/4		CLC01	3H1
CLC11	O	008	3/4		CLC11	3H1
CLK	I	305	1/3		CLKO	2A7
DV.FILL1	O	110	3/2		DV.FILL1	3H0
ENOTO	O	109	3/3		ENDTO	3H5
ERO	OT	304	2/1		ERO	2H0
GPRO	I	019	2/1		GPRO	2A6
GPO	OT	117	4/4,(2)7/1		GPO	2H6
	I		1/1,2/1			
GRDB	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INF000	OT	003	1/1		RT.ADRA0	2H5
	I	013	1/1		INF000	2A1
INF010	OT	016	1/1		IDEN0	2H8
	OT	100	1/1		RT.ADRB0	2H6
	I	113	1/1		INF010	2A1
INF020	I	014	1/1		INF020	2A1
INF030	OT	002	1/1		RT.ADRC0	2H6
	I	114	1/1		INF030	2A1
INF040	I	012	1/1		INF040	2A1
INF050	I	112	1/1		INF050	2A0
INF060	OT	101	1/1		INF060	3H3
INF070	OT	102	1/1		INF070	3H3
INF080	OT	201	1/1		INF080	3H2
INF090	OT	315	1/1		INF090	3H8
	I	217	1/1		INF090	3A7
INF100	OT	314	1/1		INF100	3H8
	I	216	1/1		INF100	3A7
INF110	OT	214	1/1		INF110	3H8
	I	011	1/1		INF110	3A6
INF120	OT	213	1/1		INF120	3H7
	I	313	1/1		INF120	3A6
INF130	OT	306	1/1		INF130	3H9
	I	007	1/1		INF130	3A0
INF140	OT	206	1/1		INF140	3H9
	I	106	1/1		INF140	3A0
INF150	OT	300	1/1		INF150	3H2
	I	006	1/1		INF150	3A0
INITO	I	107	1/3		INITO	2A1
INTPO	OT	017	2/1		INTPO	2H8
LDITR1	O	203	3/3		LDITR1	3H5
LOPCKDO	I	318	3/2		LDPCKDO	2A6
LOADO	O	215	3/3		LOADO	3H7
MRSTA1	O	204	3/2		MRSTA1	3H0
PE1	I	001	3/2		PE1	2A0
RCO	I	118	1/3		RCO	2A2

SYMBOL NO. 1 (CONT)

BUFFER - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-A	05-31	JK10	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
RDO	I	115	1/3		RDO	2A3
SDO	I	018	1/3		SDO	2A2
SSTO	I	116	1/3		SSTO	2A3
ST.CLKO	O	108	3/2		ST.CLKO	2H1
STFILLO	I	104	3/2		STFILLO	3A2
STUFFO	O	212	3/2		STUFFG	3H6
SWB1	O	009	3/2		SWB1	3H4
SYNCO	OT	103	2/1		SYNCO	2H2
TG.SEQ1	O	010	3/2		TG.SEQ1	3H5
UNLOADO	O	209	3/2		UNLOADO	3H6
WAITO	OT	015	2/1		WAITO	2H4
1ACTO	I	208	3/2		1ACTO	3A9

SYMBOL NO. 2

BUFFER - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-B	05-29	JK11	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
BACRO	I	018	3/4		BACRO	3A2
BCLK	O	116	2/1		BCLK	2H7
BLK.CBR1	O	007	3/1		BLK.CBR1	3H5
BOFLO	O	017	2/1,3/1		BOFLO	3H4
			4/3,(2)7/1			
BRO	O	015	3/1,(2)7/1		BRO	3H6
BSHPO	I	019	4/3		BSHPO	2A9
BUSYO	O	100	3/1		BUSYO	2H3
C.BR1	I	013	3/1		C.BR1	3A1
C.STC1	I	012	3/1		C.STC1	2A5
CLKITRO	O	003	3/3		CLKITRO	2H3
DV.FILL1	I	115	3/1		DV.FILL1	2A8
FILLO	I	016	4/3		FILLO	2A8
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
I16BC1	I	105	3/4		I16BC1	3A1
LDPCKDO	O	010	3/1		LOPCKDO	2H1
MRSTA1	I	014	3/1		MRSTA1	2A5
OFLCLK1	O	103	3/4		OFLCLK1	2H2
ONLCLKO	O	113	3/4		ONLCLKO	3H3
PE1	O	111	3/1		PE1	2H0
PPEHO	I	002	3/3		PPEHO	2A0
PPELO	I	102	3/3		PPELO	2A0
SDINO	OT	117	4/3,(2)7/2		SDINO	3H0
	I		2/1,3/4			
SDDTO	I	118	3/4		SDDTO	3A0
SHIFT1	O	004	3/3		SHIFT1	2H4
ST.CLKO	I	101	3/1		ST.CLKO	2A6

SYMBOL NO. 2 (CONT)

BUFFER - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-B	05-29	JK11	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
STFILLO	O	011	3/1		STFILLO	2H9
STUFFO	I	107	3/1		STUFFO	2A0
SWB1	I	112	3/1		SWB1	3A5
TG.SEQ1	I	104	3/1		TG.SEQ1	2A2
UNLOADO	I	001	3/1		UNLOADO	2A0
1ACTO	O	114	3/1,3/4		1ACTO	3H4

SYMBOL NO. 3

BUFFER - C

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-C	05-28	JK12	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		115			LDD1	2G9
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
-17.20V	OT	018	3/3		-17.20V	2G9
	OT	118			-17.20V	2G9
	I		3/4			
CLKITRO	I	015	3/2		CLKITRO	2A3
ENDTO	I	104	3/1		ENDTO	2A0
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INFPHO	OI	101	1/1		INFPHO	2H3
INFPLO	OI	005	1/1		INFPLO	2H6
INF000	OI	116	1/1		INF000	2H6
INF010	OI	216	1/1		INF010	2H6
INF020	OI	016	1/1		INF020	2H5
INF030	OI	315	1/1		INF030	2H5
INF040	OI	113	1/1		INF040	2H4
INF050	OI	215	1/1		INF050	2H4
INF060	OI	013	1/1		INF060	2H4
INF070	OI	214	1/1		INF070	2H4
INF080	OI	006	1/1		INF080	2H2
INF090	OI	207	1/1		INF090	2H2
INF100	OI	105	1/1		INF100	2H2
INF110	OI	305	1/1		INF110	2H2
INF120	OI	003	1/1		INF120	2H1
INF130	OI	203	1/1		INF130	2H1
INF140	OI	102	1/1		INF140	2H1
INF150	OI	301	1/1		INF150	2H0
LDDO	O	017	3/4		LDDO	2G9
LDITR1	I	004	3/1		LDITR1	2A6
LOADO	I	106	3/1		LOADO	2A7
PN48	I	217	6/3		PN48	2A9
	I	317	6/3		PN48	2A9
PPEHO	O	103	3/2		PPEHO	2H3
PPELO	O	114	3/2		PPELO	2H7
SDITRO		002	3/4		SDITRO	2A0
SHIFT1		014	3/2		SHIFT1	2A3

SYMBOL NO. 4

BUFFER - D

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
BUF-D	05-27	JK13	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		013			IBCC1	2H5
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
-17.20V	I	018	3/3		-17.20V	2A6
	I	117	3/3		-17.20V	2A6
BACRO	O	107	2/1,3/2		BACRO	2H5
			4/3,(2)7/1			
BA16CRO	O	006	2/1		BA16CRO	2H2
CLC01	I	012	3/1		CLC01	2A0
CLC11	I	115	3/1		CLC11	2A7
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
I16BC1	O	016	3/2		I16BC1	2H3
LDDO	I	014	3/3		LDDO	2A4
OFLCLK1	I	210	3/2		OFLCLK1	2A2
ONLCLKO	I	309	3/2		ONLCLKO	2A2
SDINO	I	015	3/2		SDINO	2A3
SDITRO	O	114	3/3		SDITRO	2H6
SDOTO	O	208	2/1,3/2		SDOTO	2H7
			4/3,(2)7/2			
1ACTO	I	116	3/2		1ACTO	2A3

PART OF FS 3
SYMBOL(S) 1 2 3 4

TAPE DATA CONTROLLER

DWG SIZE	ISSUE
C2	5AC

BELL LABORATORIES
SD-1C904-01
B3CA

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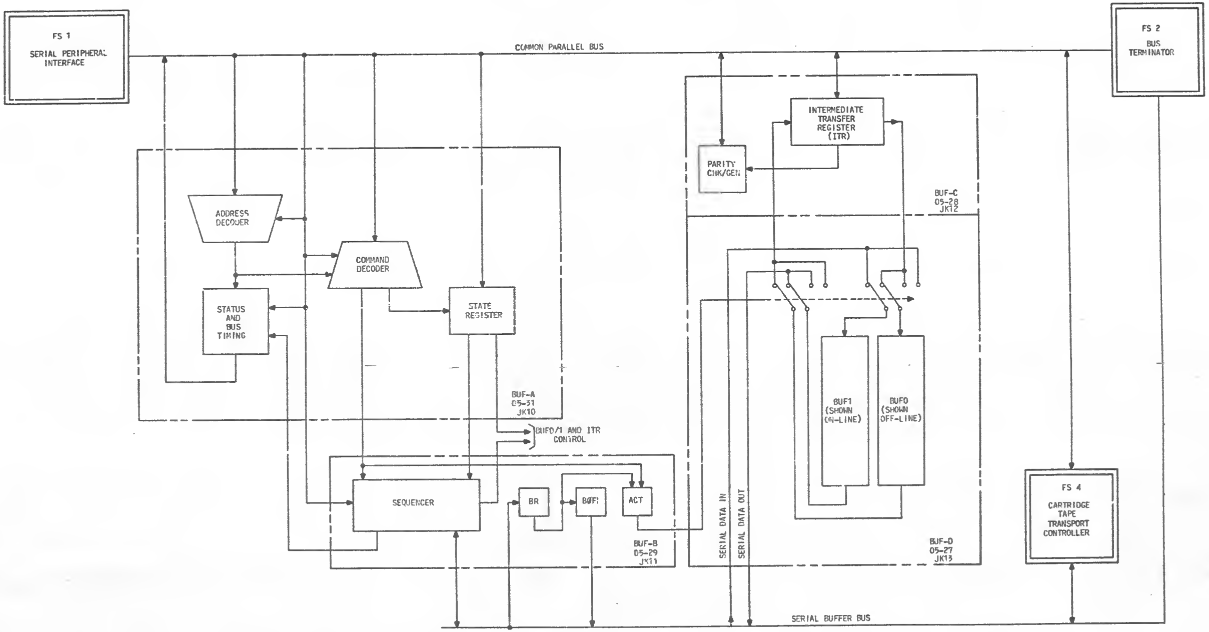
07/13/77

PART OF FS 3

BUFFER

COMPOSITE DIAGRAM I

FUNCTIONAL BLOCK DIAGRAM OF BUFFER



PART OF FS 3
COMPOSITE DIAGRAM 1

TAPE DATA CONTROLLER	DWG SIZE 65	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GA

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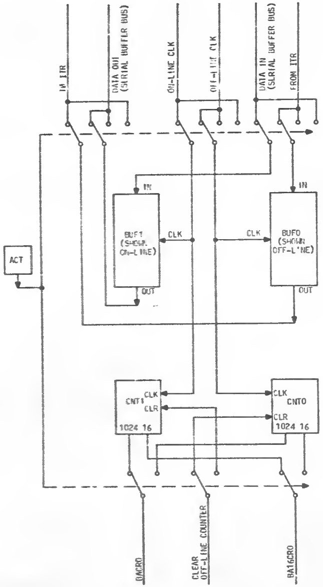
E - 7521 (12 - 73)

PART OF FS 3

BUFFER

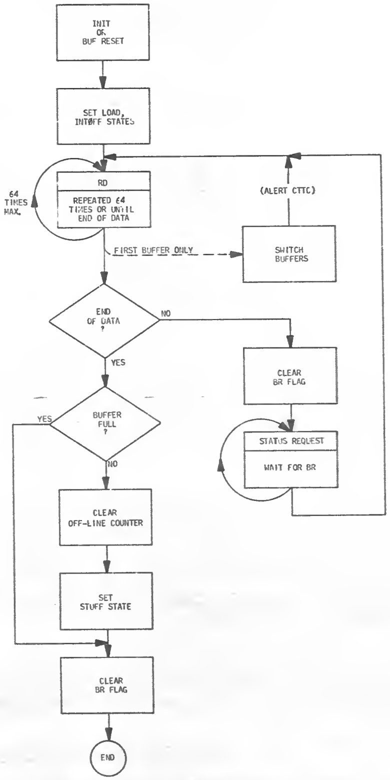
COMPOSITE DIAGRAM 2

BUFFER SWITCH BLØCK DIAGRAM; CØMMAND SEQUENCE FLØWCHARTS



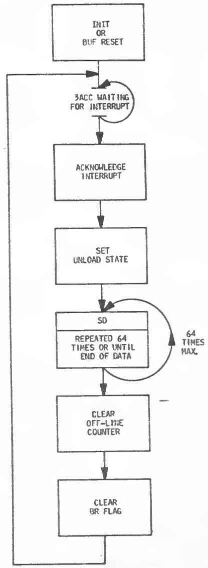
BUFFER SWITCH BLØCK DIAGRAM

FIG. 1



EXAMPLE OF A BUFFER COMMAND SEQUENCE 3ACC TO CTTC BLOCK TRANSFER

FIG. 2



EXAMPLE OF A BUFFER COMMAND SEQUENCE CTTC TO 3ACC BLOCK TRANSFER

FIG. 3

PART OF FS 3
CØMPØSITE DIAGRAM 2

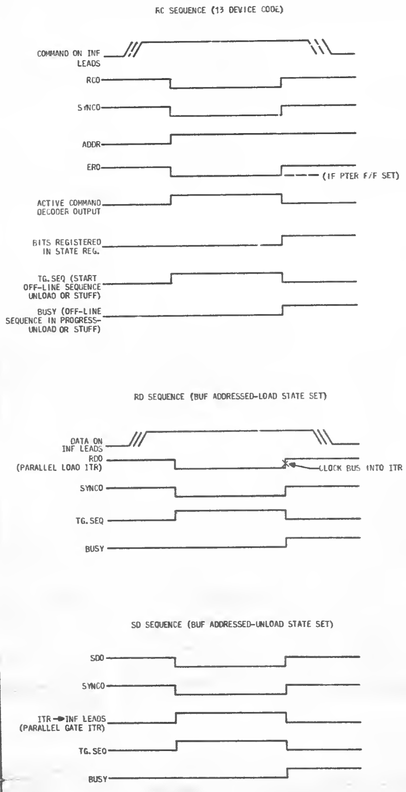
TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GB

PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 3

TIMING DIAGRAMS FØR CØMMØN PARALLEL BUS COMMUNICATIØN AND ØFF - LINE SEQUENCING


RC SEQUENCE (13 DEVICE CODE)

COMMAND ON INF LEADS
RCO
SYNCO
ADDR
ERO
(IF PTER F/F SET)
ACTIVE COMMAND DECODER OUTPUT
BITS REGISTERED IN STATE REG.
TG. SEQ (START OFF-LINE SEQUENCE UNLOAD OR STUFF)
BUSY (OFF-LINE SEQUENCE IN PROGRESS-UNLOAD OR STUFF)

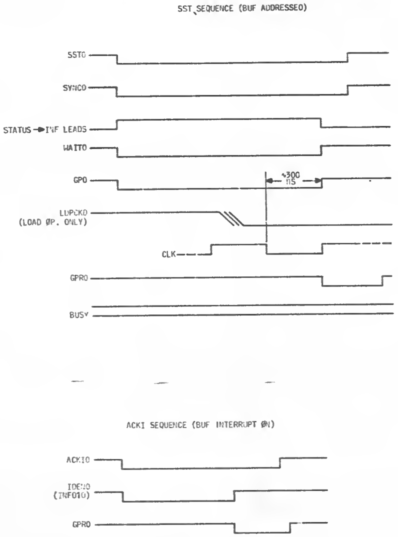
RD SEQUENCE (BUF ADDRESSED-LOAD STATE SET)

DATA ON INF LEADS
RDO (PARALLEL LOAD ITR)
CLOCK BUS INTO ITR
SYNCO
TG. SEQ
BUSY

SD SEQUENCE (BUF ADDRESSED-UNLOAD STATE SET)

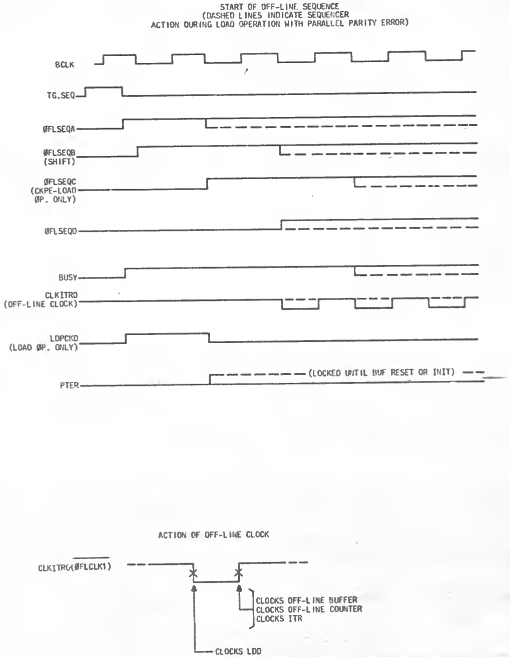
SDO
SYNCO
ITR → INF LEADS (PARALLEL GATE ITR)
TG. SEO
BUSY

FIG. 4


SST SEQUENCE (BUF ADDRESSED)

ACKI SEQUENCE (BUF INTERRUPT ØN)

FIG. 5


START OF OFF-LINE SEQUENCE (DASHED LINES INDICATE SEQUENCER ACTION DURING LOAD OPERATION WITH PARALLEL PARITY ERROR)

ACTION OF OFF-LINE CLOCK

FIG. 6

PART ØF FS 3
CØMPØSITE DIAGRAM 3

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GC

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PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 4

0FF - LINE SHIFTING - L0AD OR UNL0AD OPERATI0N

LOAD OR UNLOAD OPERATION SHIFTING

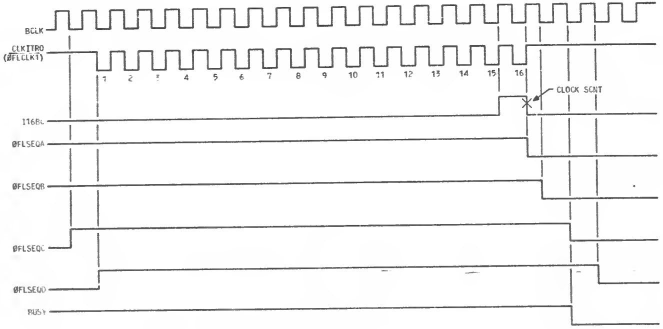


FIG. 7

PART 0F FS 3
C0MP0SITE DIAGRAM 4

TAPE DATA CONTROLLER

DWG SIZE 6S

ISSUE 2A

BELL LABORATORIES

SD-IC904-01

B3GD

PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 5

OFF-LINE SHIFTING - STUFF OPERATION

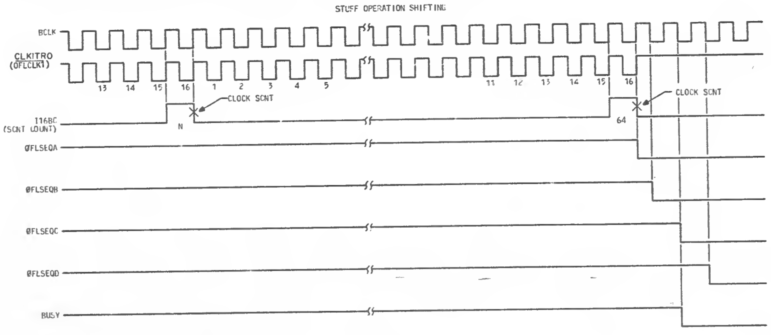


FIG. 8

PART OF FS 3
COMPOSITE DIAGRAM 5

TAPE DATA CONTROLLER ②

DWG SIZE 6S

ISSUE 2A

BELL LABORATORIES

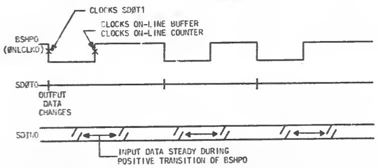
SD-1C904-01

B3GE

PART OF FS 3
BUFFER

COMPOSITE DIAGRAM 6
ON - LINE SHIFTING

ACTION OF ON-LINE CLOCK



ON-LINE SHIFTING
(DASHED LINES INDICATE ACTION LEADING TO OR RESULTING FROM OVERFLOW)

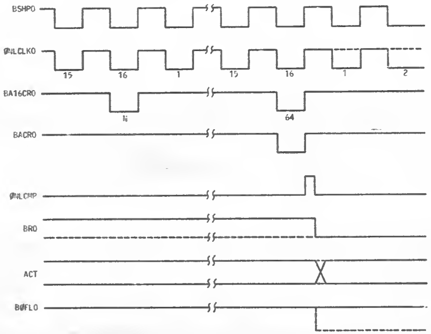


FIG. 9

PART ØF FS 3
CØMPØSITE DIAGRAM 6

TAPE DATA CONTROLLER ②

DWG SIZE 6S

ISSUE 2A

BELL LABORATORIES

SD-1C904-01

B3GF

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PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 7

ON - LINE SHIFTING - FILL OPERATION

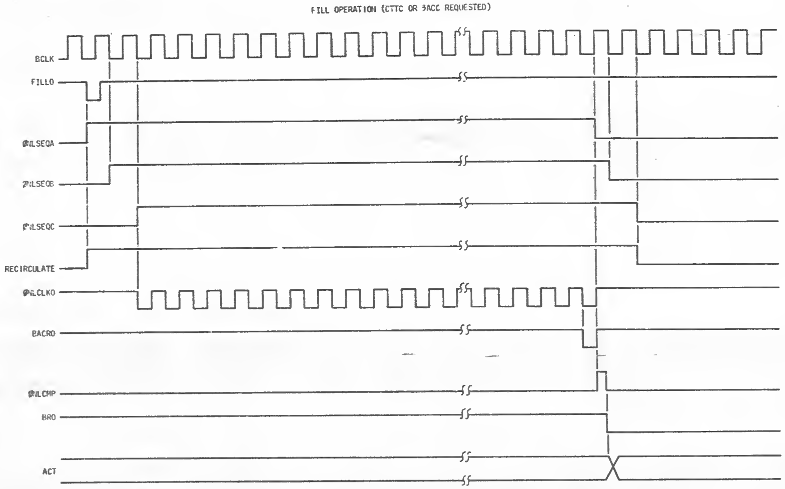

FIG. 10

PART OF FS 3
COMPOSITE DIAGRAM 7

TAPE DATA CONTROLLER ②	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GG

E - 7621 (12 - 73)

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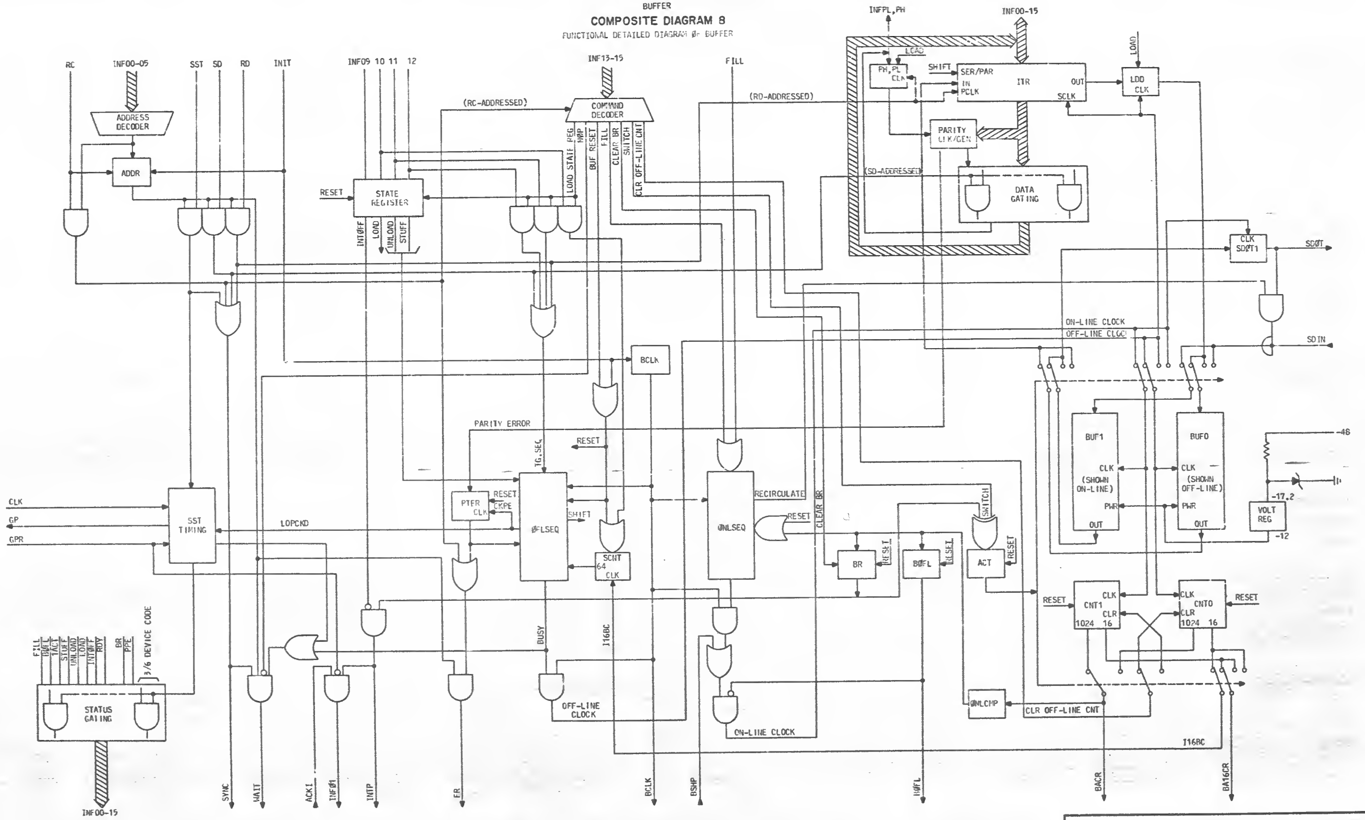
PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 8

FUNCTIONAL DETAILED DIAGRAM OF BUFFER



TAPE DATA CONTROLLER

DWG SIZE	65
ISSUE	2A

BELL LABORATORIES | SD-IC904-01 | 83GH

PART OF FS 3
COMPOSITE DIAGRAM 8

E-7002 (12-73)

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PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 9

GENERAL INFØRMATION AND DESCRIPTIØN OF BUFFER

1. GENERAL INFORMATION

THE BUFFER UNIT (BUF) IS A TEMPORARY SERIAL MEMORY DEVICE FOR BUFFERING DATA TRANSFERS BETWEEN THE 3ACC AND SERIAL DEVICES ON THE TDC COMMON PARALLEL BUS. BUF IS ESSENTIALLY BUILT AROUND TWO 1024-BIT SHIFT REGISTERS (BUFO,BUF1), WHICH ARE MAINTAINED IN OPPOSITE BUT SWITCHABLE ON-LINE/OFF-LINE STATES. AN ON-LINE BUFFER IS THAT SHIFT REGISTER WHICH IS CONNECTED TO THE SERIAL BUFFER BUS PRESENTLY SERVING THE CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC). AN OFF-LINE BUFFER IS THAT SHIFT REGISTER WHICH IS CONNECTED INDIRECTLY (THROUGH A SERIAL/PARALLEL CONVERTER) TO THE COMMON PARALLEL BUS AND MAY BE SERVICED BY THE 3ACC. THE DUAL BUFFER STRUCTURE DESCRIBED ALLØWS THE 3ACC TØ SERVICE THE ØFF - LINE BUFFER AT ITS CONVENIENCE WHILE A CTTC/ON-LINE BUFFER SERIAL CONVERSATION PROGRESSES AT THE CTTC DATA RATE. THE ON-LINE/OFF-LINE BUFFER STATUS SWITCHES AT THE COMPLETION OF EACH 1024-BIT DATA TRANSFER ON THE SERIAL BUS, TRANSPARENTLY PROVIDING THE CTTC WITH A FRESH BUFFER WHILE FLAGGING AN OFF-LINE BUFFER SERVICE REQUEST. BUF INCLUDES FEATURES FOR TRANSFERRING VARIABLE LENGTH DATA BLOCKS IN 16-BIT WORD INCREMENTS.

THE BUF FUNCTIONAL PARTITION DIRECTLY CORRESPONDS TO THE PHYSICAL PARTITION OF THE CIRCUIT ONTO FOUR BOARDS, AS SHOWN IN COMPOSITE DIAGRAM 1. BUF-A (JK10) INTERFACES WITH THE COMMON PARALLEL BUS AND PERFORMS BUF ADDRESS AND COMMAND DECODING. BUF-C (JK12) PROVIDES THE SERIAL/PARALLEL CONVERSION CAPABILITY NECESSARY TO TRANSFER DATA BETWEEN THE COMMON PARALLEL BUS AND THE 1024-BIT SHIFT REGISTERS LOCATED ON BUF-D (JK13). BUF-C ALSO INCLUDES PARITY CHECKING AND GENERATION CIRCUITS. BUF-B (JK11) PERFORMS THE SEQUENCING INVOLVED IN STEERING DATA THROUGH THE BUFFER.

2. GENERAL DESCRIPTION

2.1 ADDRESS DECODING

BUF RESIDES AS A PERIPHERAL DEVICE ON THE COMMON PARALLEL BUS FOR WHICH THE COMMUNICATIONS PROTOCOL HAS BEEN DESCRIBED IN FS 1 AND FS 2. BUF IS ASSIGNED DEVICE CODE 13. THE APPEARANCE OF THIS DEVICE CODE ON THE SIX LOW-ORDER BUS INFORMATION LEADS, ACCOMPANYING AN ACTIVE RC BUS CONTROL LEAD, ADDRESSES BUF AND ENABLES THE DECODING OF COMMAND INFORMATION ON THE TEN HIGH-ORDER BUS INFORMATION LEADS. ONCE SELECTED, BUF LATCHES INTO AN ADDRESSED STATE, TURNING ITSELF ON TO FURTHER PARALLEL BUS COMMUNICATION. BUF IS DESELECTED UPON THE RECEPTION OF AN RC SIGNAL ACCOMPANIED BY OTHER THAN A 13 DEVICE CODE.

2.2 COMMAND DECODING

CODED COMMAND INFORMATION IS BROUGHT INTO THE COMMAND DECODER ON THE THREE HIGHEST ORDER BUS INFORMATION LEADS. THE DECODER RESPONDS BY DRIVING CONTROL CIRCUITS WHICH PERFORM OR INITIATE THE ACTION SPECIFIED BY THE CODE. THE EIGHT 3-BIT CODES FOLLOW:

OCTAL CODE (INF15-INF13)	ACTION
0	NØP. INDICATES A STATUS REQUEST WILL FOLLOW.
1	CLEARS THE BR (BUFFER READY) FLAG, INDICATING THE 3ACC HAS COMPLETED SERVICING THE OFF-LINE BUFFER. (THE BR IS RAISED TO REQUEST 3ACC SERVICING OF THE OFF-LINE BUFFER.)
2	LOADS THE 4-BIT STATE REGISTER FROM PARALLEL BUS LEADS INF09 THROUGH INF12.
3	INITIATES AN ON-LINE BUFFER FILL OPERATION. A FILL OPERATION CAUSES THE DATA QUEUE IN THE ON-LINE BUFFER TO BE STEPPED TO THAT BUFFER'S OUTPUT IF NOT ALREADY THERE.
4	NOT USED.
5	CLEARS THE COUNTER ASSOCIATED WITH THE OFF-LINE BUFFER.
6	SWITCHES THE ON-LINE/OFF-LINE STATUS OF BUFO AND BUF1.
7	RESETS BUF CIRCUITS. BUF REMAINS IN AN ADDRESSED STATE.

THE STATE REGISTER BIT DESIGNATIONS FOLLOW. THE FIRST THREE ARE USED TO SELECT DIFFERENT OFF-LINE BUFFER OPERATIONAL MODES.

INF LEAD	STATE REGISTER BIT
12	STUFF. A STUFF OPERATION CAUSES THE DATA QUEUE IN THE OFF-LINE BUFFER TO BE STEPPED TO THAT BUFFER'S OUTPUT IF NOT ALREADY THERE.
11	UNLOAD. AN UNLOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE OFF-LINE BUFFER TO THE 3ACC.
10	LOAD. A LOAD OPERATION IS DEFINED BY A 16-BIT DATA TRANSFER FROM THE 3ACC TO THE OFF-LINE BUFFER.
9	INTØFF. INHIBITS BUF ASSERTION OF THE PARALLEL BUS INTERRUPT LEAD INTPO. (INTPO IS OTHERWISE ASSERTED BY A RAISED BR FLAG.)

2.3 OFF-LINE BUFFER OPERATIONS

THE INTERMEDIATE TRANSFER REGISTER (ITR) PERFORMS SERIAL/PARALLEL CONVERSION IN ALL DATA TRANSFERS BETWEEN THE OFF-LINE BUFFER AND THE 3ACC. IN A LOAD OPERATION, THE ITR ACCEPTS DATA APPEARING ON THE 16-PARALLEL BUS INFORMATION LEADS. THE BUS PARITY BITS ARE LOADED INTO AN AUXILIARY 2-BIT REGISTER. THE PARALLEL LOADING OF THE ITR OCCURS IN RESPONSE TO A SIGNAL ON THE BUS CONTROL LEAD ROO (NOTE THAT BUF MUST BE ADDRESSED). PARITY TREES HANGING ON THE ITR OUTPUTS MATCH THE PARALLEL DATA PARITY WITH THE REGISTERED PARITY BITS TO CHECK FOR BUS PARITY ERRORS. BARRING THE OCCURRENCE OF A PARALLEL PARITY ERROR, THE ITR ENTERS A SERIAL SHIFT MODE AND THE 16 DATA BITS ARE CLOCKED INTO THE OFF-LINE BUFFER UNDER CONTROL OF THE SEQUENCER ON BUF-B. A COUNTER ASSOCIATED WITH THE OFF-LINE BUFFER SIGNALS THE SEQUENCER WHEN 16 BITS HAVE BEEN TRANSFERRED. A DETECTED PARALLEL PARITY ERROR WILL INHIBIT SERIAL SHIFTING OF THE ITR.

IN AN UNLOAD OPERATION, THE SEQUENCER MOVES 16 BITS FROM THE OFF-LINE BUFFER INTO THE ITR (WHICH IS IN A SERIAL SHIFT MODE). THE PARITY TREES GENERATE ODD PARITY OVER THE HIGH AND LOW BYTES OF THE DATA WORD. THE DATA AND PARITY ARE GATED ONTO THE PARALLEL BUS BY BUS CONTROL SIGNAL SOO.

THE ITR IS NOT INVOLVED IN A STUFF OPERATION. STUFF SEQUENCING CAUSES ZEROES TO BE SHIFTED INTO THE OFF-LINE BUFFER TO PAD OUT A BUFFER CONTAINING LESS THAN 1024 DATA BITS.

2.4 ON-LINE BUFFER OPERATIONS

THE ON-LINE BUFFER FORMS THE DATA PORT OF A SERIAL BUFFER BUS WHICH PRESENTLY SERVES ONLY THE CTTC. THE SERIAL BUFFER BUS INCLUDES SEVERAL CONTROL AND STATUS LEADS WHICH ALLOW THE CTTC TO CONTROL THE MOVEMENT OF DATA INTO AND OUT OF THE ON-LINE BUFFER WITHOUT INTERFERING BUF OFF-LINE OPERATIONS OR EVEN REQUIRING BUF TO BE ADDRESSED. IN PARTICULAR, THE CTTC-DRIVEN BUFFER SHIFT PULSE CONTROL LEAD (BSHPO) DIRECTLY CLOCKS THE ON-LINE BUFFER. A DATA BIT APPEARING ON THE SERIAL DATA INPUT LEAD IS CLOCKED INTO THE BUFFER BY BSHPO WHILE A DATA BIT AT THE BUFFER OUTPUT IS PRESENTED ON THE SERIAL DATA OUTPUT LEAD. A COUNTER ASSOCIATED WITH THE ON-LINE BUFFER PROVIDES A MARKER PULSE (BA16CRO) ON THE SERIAL BUS WHICH INDICATES THE COMPLETION OF EACH 16-BIT ON-LINE DATA TRANSFER. A 1024-BIT MARKER PULSE (BACRO) IS ALSO AVAILABLE TO DEVICES ON THE SERIAL BUFFER BUS.

A FILL OPERATION CAN BE INITIATED BY THE CTTC (VIA SERIAL BUFFER BUS LEAD FILLO) TO PAD OUT A BUFFER TO WHICH THE CTTC HAS TRANSFERRED LESS THAN 1024 BITS. FILL CAN ALSO BE INITIATED BY A 3ACC COMMAND FOR MAINTENANCE PURPOSES. IN EITHER CASE, THE ON-LINE BUFFER IS ADVANCED BY THE BUF SEQUENCER UNTIL BACRO IS DETECTED. THE ON-LINE BUFFER MAY BE RECIRCULATED OF ØNES PADDED DURING A FILL OPERATION, DEPENDING ON THE STATE OF THE SERIAL DATA INPUT LEAD.

2.5 BUFFER SWITCHING

DATA AND CLOCK INFORMATION IS STEERED TO OR FROM THE PROPER BUFFER BY MULTIPLEXER SWITCHING DIRECTLY CONTROLLED BY THE STATE OF THE ACT F/F. BUFFER INITIALIZATION FORCES ACT INTO STATE SHOWN IN FIGURE 1 (SHT B3GB) WITH BUFØ OFF - LINE AND BUF1 ON-LINE. COUNTER CNTO (ASSOCIATED WITH BUFO) IS CONFIGURED TO THE OFF-LINE CLOCK ALONG WITH BUFO WHILE CNT1 AND BUF1 ARE CONFIGURED TO THE ON-LINE CLOCK SOURCE. TOGGLING ACT RESULTS IN A REVERSAL OF THE ON-LINE/OFF-LINE STATUS OF BUFO,BUF1, AND THEIR ASSOCIATED COUNTERS. SUBSEQUENT CHANGES IN THE STATE OF THE ACT F/F YIELD SIMILAR BUFFER REVERSALS. THE BR FLAG IS SET BY THE ON-LINE BUFFER COUNTER BACRO SIGNAL AND INDICATES THAT THE ON-LINE BUFFER HAS BEEN CLOCKED 1024 TIMES AND NOW REQUIRES SERVICING BY THE 3ACC. RAISING THE BR FLAG NORMALLY ASSERTS THE PARALLEL BUS INTERRUPT LEAD (INTPO) UNLESS STATE REGISTER BIT INTOFF IS SET. RAISING THE BR FLAG ALSO TOGGLES THE ACT F/F, SWITCHING THE BUFFERS. THE 3ACC MAY THEN SERVICE THE NEW OFF-LINE BUFFER AND RETIRE THE BR FLAG UPON COMPLETION. IF THE 3ACC DOES NOT MANAGE TO RETIRE THE BR FLAG BEFORE CURRENT ON-LINE BUFFER OPERATIONS ARE COMPLETE (INDICATED BY BACRO), A BUFFER SWITCH WILL NOT OCCUR, THE BØFL F/F (BUFFER OVERFLOW) IS SET, AND ALL SUBSEQUENT CLOCK SIGNALS TO THE ON-LINE BUFFER ARE CUT OFF. THE STRANDED ON-LINE BUFFER MAY BE BROUGHT OFF-LINE BY A 3ACC COMMAND TO SWITCH BUFFERS, TOGGLING ACT THROUGH THE COMMAND DECODER. DATA IN THIS BUFFER MAY THEN BE RETRIEVED BY SUCCESSIVE UNLOAD OPERATIONS.

2.6 STATUS REPLIES

BUF STATUS, ACCOMPANIED BY A 13 DEVICE CODE, IS REPORTED ON THE PARALLEL BUS IN RESPONSE TO A SST CONTROL SIGNAL. THE STATUS BIT DESIGNATIONS FOLLOW:

INF. BIT	STATUS BIT	STATUS WHEN ACTIVE
15	FILL	FILL OPERATION IN PROGRESS.
14	BØFL	BUFFER OVERFLOW CONDITION EXISTS.
13	1ACT	BUF1 IS PRESENTLY ACTIVE (ON-LINE).
12	STUFF	STATE REGISTER STUFF BIT SET AND STUFF OPERATION INITIATED.
11	UNLOAD	STATE REGISTER UNLOAD BIT SET AND UNLOAD OPERATION INITIATED.
10	LOAD	STATE REGISTER LOAD BIT SET AND ITR IN PARALLEL LOAD MODE.
9	INTØFF	INTERRUPT LEAD DISABLED.
B	RDY	NO OFF-LINE BUFFER SEQUENCING OPERATIONS ARE CURRENTLY IN PROGRESS.
7	BR	OFF-LINE BUFFER READY FOR SERVICING.
6	PPE	PARALLEL PARITY ERROR ENCOUNTERED.

BITS 5-0 CONTAIN THE 13 DEVICE CODE. BUF BUS TIMING LOGIC USES PARALLEL BUS LEAD GPO TO REQUEST PARITY GENERATION OVER THE STATUS WORD BY THE BUS TERMINATOR.

2.7 DATA BLOCK TRANSFER COMMAND SEQUENCES

2.7.1 BLOCK TRANSFERS FROM 3ACC TO CTTC

AN EXAMPLE BUF COMMAND SEQUENCE FOR MOVING A BLOCK OF DATA FROM THE 3ACC TO THE CTTC IS FLOWCHARTED IN FIGURE 2 AND DESCRIBED BELOW.

BUF SHOULD BE INITIALIZED INTO A KNOWN STATE VIA A TDC SYSTEM INITIALIZATION SIGNAL ON PARALLEL BUS LEAD INITO OR BY A BUF RESET COMMAND. THE LOAD BIT MUST THEN BE SET IN THE STATE REGISTER TO ENABLE THE REGISTRATION OF PARALLEL PARITY BITS. THE INTØFF BIT IS ALSO SET IN THIS EXAMPLE. A SERIES OF LOAD OPERATIONS TRIGGERED BY RD COMMANDS BEGINS, EACH RD MOVING A 16-BIT DATA WORD THROUGH THE ITR AND INTO BUFO. WHEN THE 64-WORD CAPACITY OF BUFO IS REACHED (ASSUMING A DATA BLOCK GREATER THAN 64 WORDS FOR SIMPLICITY), BUFO IS SWITCHED ON-LINE AND THE CTTC IS ALERTED THAT IT IS TO RECEIVE A DATA BLOCK. LOAD OPERATIONS CONTINUE ON BUF1. WHEN BUF1 HAS BEEN LOADED TO ITS 64-WORD CAPACITY, OFF-LINE BUFFER OPERATIONS ARE SUSPENDED AND BUF STATUS REQUESTS MUST BE PERIODICALLY MADE TO CHECK THE STATE OF THE BR FLAG SINCE THE INTERRUPT FACILITY IS INHIBITED.

THE CTTC BEGINS TO DEPLETE THE ON-LINE BUFFER. A STATUS REPLY INDICATING THAT THE BR FLAG HAS BEEN RAISED IMPLIES A BUFFER SWITCH HAS OCCURRED AND OFF-LINE LOADING OPERATIONS CAN CONTINUE. AS BUF COMPLETES THE LOADING OF AN OFF-LINE BUFFER, THE BR FLAG IS CLEARED. IT IS IMPORTANT THAT THE OFF-LINE LOADING OF THE SECOND BUFFER BE COMPLETED BEFORE THE FIRST BR FLAG IS RAISED; OTHERWISE, AN OVERFLOW SITUATION OCCURS (A PREMATURE BUFFER SWITCH) BUT BØFL DOESN'T GET SET.

FOR DATA BLOCKS WHICH ARE NOT MULTIPLES OF 64 WORDS, THE FINAL BUFFER IS PARTIALLY LOADED, THE COUNTER ASSOCIATED WITH THAT OFF-LINE BUFFER IS CLEARED TO MARK THE NUMBER OF DATA WORDS IN THE BUFFER, A STUFF OPERATION IS INITIATED, AND THE BR FLAG IS CLEARED AT THE COMPLETION OF THE STUFF.

2.7.2 BLOCK TRANSFERS FROM CTTC TO 3ACC

AN EXAMPLE BUF COMMAND SEQUENCE FOR MOVING A BLOCK OF DATA FROM THE CTTC TO THE 3ACC IS FLOWCHARTED IN FIGURE 3. BUF SHOULD BE INITIALIZED AT THE START. AN ACKNOWLEDGED BUF INTERRUPT INDICATES THAT THE BR HAS BEEN RAISED AND BUF1 HAS JUST BEEN SWITCHED OFF-LINE FOR SERVICING. THE UNLOAD BIT IS SET IN THE STATE REGISTER WHICH ADVANCES THE FIRST DATA WORD INTO THE ITR. AN SD COMMAND WILL GATE THE ITR ONTO THE PARALLEL BUS AND ADVANCE THE NEXT WORD INTO THE ITR. 64 SD COMMANDS ARE REQUIRED TO MOVE A FULL BUFFER OF DATA TO THE 3ACC, AFTER WHICH THE OFF-LINE COUNTER IS CLEARED. THE BR FLAG IS RETIRED AND THE 3ACC WAITS FOR THE NEXT INTERRUPT. NOTE THAT THE UNLOAD STATE MUST BE SET EACH TIME A BUFFER IS TO BE DUMPED TO THE 3ACC IN ORDER TO GET THE FIRST WORD OF EACH BUFFER INTO THE ITR.

THE CTTC MUST REQUEST A FILL OPERATION ON THE LAST ON-LINE BUFFER IF THE BLOCK LENGTH IS NOT A MULTIPLE OF 64 WORDS.

3. SEQUENCE INFORMATION

COMPOSITE DIAGRAM B PRØVIDES A FUNCTIØNAL REFERENCE DRAWING FOR TIMING DIAGRAMS THAT FOLLOW, AND AS SUCH IS NOT MEANT TO OFFER AN ACCURATE GATE LEVEL DESCRIPTION. THE BUF CPS DRAWINGS SHOULD BE REFERENCED FOR GATE LEVEL RESOLUTION. A TIMING DIAGRAM MNEMONIC ENDING IN 0 OR 1 DIRECTLY CORRESPONDS TO A PHYSICAL CIRCUIT LEAD WHOSE LOGIC POLARITY WILL BE CORRECTLY INDICATED ON THE DIAGRAM.

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GJ

PART OF FS 3

BUFFER

COMPOSITE DIAGRAM 10

BUFFER SEQUENCE INFØRMATIØN

3.1 PARALLEL BUS COMMUNICATIONS

BUF RECEIVES A COMMAND FROM THE 3ACC VIA THE RC SEQUENCE SHOWN IN FIGURE 4 (SHT B3GC). THE BUF DEVICE CODE AND COMMAND INFORMATION APPEARS ON THE BUS BEFORE THE LEADING EDGE OF RCO, ALLOWING ADDRESS AND COMMAND DECODER SET UP TIME. THE LEADING EDGE OF RCO WILL LATCH THE ADDR F/F AND ENABLE ONE OF THE EIGHT COMMAND DECODER OUTPUTS. BUF RETURNS SYNCO AND ERO ON THE BUS AT THIS TIME TO VERIFY THAT A CONTROL SIGNAL HAS BEEN RECEIVED AND TO CHECK FOR PROPER OPERATION OF THE ERO LEAD, RESPECTIVELY. THE TRAILING EDGE OF RCO ALLOWS SYNCO TO DROP OFF. ERO WILL ALSO DROP OFF AT THIS TIME UNLESS THE PTER F/F (PARITY ERROR) HAS BEEN SET IN A PREVIOUS BUF OPERATION. IN THIS CASE, ERO WILL REMAIN ACTIVE UNTIL BUF IS RESET OR DESELECTED.

THE BUS INFORMATION WILL REMAIN STEADY FOR A PERIOD BEYOND THE TRAILING EDGE OF RCO. THIS EDGE IS INDIRECTLY USED TO CLOCK LEADS INFO9-12 INTO THE STATE REGISTER IF SUCH AN OPERATION HAS BEEN SPECIFIED BY THE COMMAND DECODER. IF THE UNLOAD OR STUFF BIT IS TO BE SET IN THE STATE REGISTER, THE COMMAND DECODER LOAD STATE REGISTER OUTPUT PRODUCES PULSE TG.SEQ WHOSE TRAILING EDGE IS USED TO TOGGLE THE FIRST ELEMENT IN AN OFF-LINE SEQUENCE TIMING CHAIN. A BUSY STATE IS ENTERED FOR THE DURATION OF THE OFF-LINE SEQUENCE INITIATED.

BUF RECEIVES DATA FROM THE 3ACC VIA RD SEQUENCES. BUF MUST BE ADDRESSED WITH THE STATE REGISTER LOAD BIT SET PRIOR TO A VALID DATA TRANSFER FROM 3ACC TO BUF. IF BUF IS NOT ADDRESSED, CONTROL SIGNALS RD, SD, OR SST ARE IGNORED. IF BUF IS ADDRESSED BUT NOT IN THE LOAD STATE, A 1-BIT BUFFERING REGISTER AT THE ITR SERIAL OUTPUT (LOD) IS HELD CLEAR PREVENTING DATA SHIFTED OUT OF THE ITR FROM REACHING THE OFF-LINE BUFFER. IN ADDITION TO THE LOCK UP OF LOD, THE AUXILIARY 2-BIT PARITY REGISTER IS ALSO HELD CLEAR, RESULTING IN A PARITY ERROR AS SOON AS AN EVEN PARITY BYTE IS REGISTERED IN THE ITR.

THE LEADING EDGE OF RDO CAUSES SYNCO TO BE RETURNED AND TG.SEQ TO BE ASSERTED. THE TRAILING EDGE OF RDO REGISTERS DATA ON THE PARALLEL BUS INTO THE ITR AND ITS ASSOCIATED PARITY REGISTER. SYNCO AND TG.SEQ DROP OFF AND THE BUSY STATE IS ENTERED FOR THE DURATION OF THE LOAD SEQUENCE.

THE 3ACC RECEIVES DATA FROM BUF VIA SD SEQUENCES. BUF MUST BE ADDRESSED WITH THE STATE REGISTER UNLOAD BIT SET PRIOR TO A VALID DATA TRANSFER. SETTING THE UNLOAD BIT PRIMES THE ITR FOR THE FIRST SD.

THE LEADING EDGE OF THE SDO CAUSES BUF TO ASSERT SYNCO AND TG.SEQ. THE ITR IS GATED ONTO THE PARALLEL BUS FOR THE DURATION OF SDO. THE TRAILING EDGE OF SDO REMOVES THE ITR FROM THE BUS AND NEGATES SYNCO. THE BUSY STATE IS ENTERED FOR THE DURATION OF THE UNLOAD SEQUENCE.

THE 3ACC REQUESTS BUF STATUS VIA THE SST SEQUENCE ON FIGURE 5. AN ADDRESSED BUF RESPONDS TO THE ASSERTION OF SSTO BY ACTIVATING SYNCO, WAITO, AND GPO AND BY GATING STATUS INFORMATION ONTO THE BUS. LDPCKD DELAYS FURTHER ACTION IN A SST WHICH FOLLOWS A RD UNTIL THE RESULTS OF THE LOAD OPERATION PARITY CHECK CAN BE REPORTED. LDPCKD IS ONLY ACTIVE IN LOAD OPERATIONS. WHEN RELEASED FROM THE DELAY, A 2-STAGE TIMING CHAIN IN THE BUF SST CIRCUIT LOOKS FOR THE NEXT NEGATIVE TRANSITION ON PARALLEL BUS CLOCK LEAD CLK AND RELEASES GPO ON THE FOLLOWING POSITIVE TRANSITION INSURING THAT GPO IS OF SUFFICIENT WIDTH TO OPERATE THE PARITY GENERATION CIRCUITS IN THE BUS TERMINATOR (BT). BT RESPONDS WITH GPRO, INSTRUCTING BUF TO REMOVE ITS STATUS AND ITS WAITO FROM THE BUS. BUF LATER REMOVES SYNCO AFTER SSTO HAS BEEN NEGATED.

THE SST EXCHANGE PROCEEDS AS DESCRIBED REGARDLESS OF THE BUSY STATUS OF BUF. THE SAME IS NOT TRUE WITH RESPECT TO RD, SD, AND RC EXCHANGES. IF A BUSY CONDITION EXISTS IN BUF, THE ASSERTION OF RDO, SDO, OR RCO RESULTS IN BUF'S ASSERTION OF WAITO. RDO, SDO, OR RCO WILL REMAIN HUNG UP IN AN ACTIVE STATE UNTIL WAITO CAN BE REMOVED. BUSY IS REMOVED AT THE COMPLETION OF AN OFF-LINE OPERATION, RELEASING WAITO AND ALLOWING THE PARALLEL BUS SEQUENCE IN PROGRESS TO CONTINUE. AN EXCEPTION TO THE ABOVE IS AN RC NOP COMMAND IN WHICH A COMMAND DECODER OUTPUT IS USED TO INHIBIT WAITO. RC NOP CAN BE USED TO ADDRESS BUF WITHOUT HANGING UP THE BUS IF BUF IS BUSY. THE ABSENCE OF THE BUSY CONDITION IS REFLECTED BY THE STATE OF THE RDY STATUS BIT.

BUF REPORTS AN INTERRUPT TO THE 3ACC WHEN THE BR FLAG IS SET AND THE STATE REGISTER BIT INTOFF IS NOT SET. ASSERTION OF BUS CONTROL LEAD ACKIO GATES BUF'S INTERRUPT IDENTIFICATION RESPONSE ONTO INFO10. THIS LEAD IS RELEASED UPON RECEPTION OF GPRO.

3.2 OFF-LINE SEQUENCER

COMPOSITE DIAGRAM 6 SHOWS BUF SEQUENCING TO BE DIVIDED BETWEEN TWO DISTINCT SEQUENCERS. THE OFF-LINE SEQUENCER ØFLSEQ HANDLES LOAD, UNLOAD, AND STUFF OPERATIONS. ØFLSEQ IS BASICALLY A FOUR ELEMENT TIMING CHAIN (ØFLSEQA-D) DRIVEN BY A FREE-RUNNING BUF CLOCK (BCLK). BCLK PROVIDES A SQUARE WAVE PULSE TRAIN WITH A NOMINAL 600 NS PERIOD.

ØFLSEQ ACTION BEGINS WITH A TG.SEQ PULSE. TG.SEQ IS DERIVED FROM SD OR RD PULSES OR RC PULSES WHICH SET THE STATE REGISTER STUFF OR UNLOAD BITS. THE TRAILING EDGE OF TG.SEQ TOGGLES ØFLSEQA WHICH THEN ENABLES THE CONSECUTIVE ACTIVATION OF TIMING CHAIN ELEMENTS ØFLSEQB-D ON SUCCESSIVE NEGATIVE TRANSITIONS OF BCLK, FIGURE 6 (SHT B3GC). A BUSY CONDITION EXISTS WHENEVER ØFLSEQA OR C ARE ACTIVATED. THE ACTIVATION OF ØFLSEQB FORCES THE ITR INTO THE SERIAL SHIFTING MODE. ØFLSEQD ENABLES AN OFF-LINE CLOCK SIGNAL (CLKITRO, ØFLCLK1) DERIVED FROM BCLK. A NEGATIVE TRANSITION OF THE OFF-LINE CLOCK SIGNAL CLOCKS THE STATE OF THE ITR SERIAL OUTPUT INTO LDD. THE FOLLOWING POSITIVE TRANSITION MOVES THE OFF-LINE BUFFER OUTPUT INTO THE ITR, CLOCKS THE STATE OF LDD INTO THE BUFFER INPUT, AND INCREMENTS THE BUFFER COUNTER.

THE SEQUENCE OF FIGURE 6 IS PERFORMED AT THE START OF ALL OFF-LINE OPERATIONS WITH THE EXCEPTION OF THE LOAD OPERATION WHICH REQUIRES THE ADDITIONAL PARITY CHECKING FUNCTION. LDPCKD (DELAYS A SST OPERATION) IS ACTIVE FROM THE POSITIVE ØFLSEQA TRANSITION TO POSITIVE ØFLSEQC TRANSITION AT WHICH TIME PARALLEL PARITY IS CHECKED. A PARITY ERROR AT THIS TIME SETS PTER F/F CAUSING THE TIMING CHAIN ELEMENTS TO SEQUENTIALLY DROP OFF AND INHIBITING ANY OFF-LINE CLOCK PULSES. ØFLSEQ IS LOCKED OFF UNTIL THE PTER F/F IS CLEARED VIA BUF RESET OR INIT. THE ABSENCE OF A PARITY ERROR AT THE ØFLSEQC TRANSITION ALLOWS ØFLSEQ TO CONTINUE THE LOAD OPERATION.

ØFLSEQD ENABLES THE SHIFTING PHASE OF AN OFF-LINE OPERATION. FIGURE 7 (SHT B3GD) SHOWS THE SHIFTING ASSOCIATED WITH A LOAD OR UNLOAD OPERATION. SIXTEEN DATA BITS ARE SERIALLY TRANSFERRED BETWEEN THE ITR AND THE OFF-LINE BUFFER BY THE OFF-LINE CLOCK. THE OFF-LINE BUFFER COUNTER GENERATES A 16-BIT CARRY PULSE, I16BC, WHOSE TRAILING EDGE TERMINATES SHIFTING AND INCREMENTS STUFF COUNTER SCNT. SCNT TALLIES THE NUMBER OF I16BC PULSES (16-BIT TRANFERS) DETECTED SINCE THE LOAD STATE WAS LAST SET. ØFLSEQ DROPS OFF AS SHOWN AT THE COMPLETION OF SHIFTING. SCNT RECYCLES TO ZERO ON THE RECEPTION OF THE 64TH I16BC PULSE.

SHIFTING IN A STUFF OPERATION (FIGURE 8 - SHT B3GE) PRØCEEDS CØNTINUOUSLY OVER 16-BIT WORD BOUNDARIES UNTIL DATA IN THE OFF-LINE BUFFER HAS BEEN RIGHT-ADJUSTED TO THE BUFFER OUTPUT, AS INDICATED BY SCNT. LDD IS HELD CLEAR DURING STUFF SHIFTING, PADDING THE OFF-LINE BUFFER WITH ALL ZEROES.

3.3 SERIAL BUFFER BUS

FOLLOWING IS A DESCRIPTION OF THE LEADS WHICH COMPRISE THE SERIAL BUFFER BUS. THESE LEADS ARE ALL TERMINATED AT THE BT.

BSHPO - BUFFER SHIFT PULSE

BSHPO IS THE PRIMARY CLOCK SOURCE FOR THE ON-LINE BUFFER. CLOCK PULSES SUPPLIED BY THE CTTC ON THIS LEAD SHIFT DATA INTO AND OUT OF THE ON-LINE BUFFER.

SDØTO - SERIAL DATA OUT

DATA SHIFTED OUT OF THE ON-LINE BUFFER APPEARS ON SDØTO FOLLOWING A NEGATIVE TRANSITION ON BSHPO, FIGURE 9 (SHT B3GF). DATA IS NOT VALID PRIOR TO THE LEADING EDGE OF THE FIRST CLOCK PULSE.

SDINO - SERIAL DATA IN

DATA IS SHIFTED INTO THE ON-LINE BUFFER FROM THIS LEAD ON THE TRAILING EDGE OF BSHPO. INPUT DATA MUST BE STEADY FOR A PERIOD BRACKETING THIS TRANSITION.

BA16CRO - BUFFER ACTIVE 16-BIT COUNTER CARRY

BA16CRO IS A MARKER PULSE GENERATED BY THE ON-LINE BUFFER COUNTER WHICH COINCIDES WITH EVERY 16TH ON-LINE CLOCK PULSE.

BACRO - BUFFER ACTIVE COUNTER CARRY

BACRO IS A MARKER PULSE GENERATED BY THE ON-LINE BUFFER COUNTER INDICATING THE ON-LINE BUFFER HAS BEEN CLOCKED 1024 TIMES.

BØFLO - BUFFER OVERFLOW

A BUFFER OVERFLOW CONDITION IS REPORTED TO THE CTTC ON BØFLO IF A BACRO PULSE OCCURS BEFORE THE BR FLAG CAN BE RETIRED. AN OVERFLOW CONDITION LOCKS OUT ON-LINE CLOCK SIGNALS.

FILLO - FILL THE ON-LINE BUFFER

THE CTTC ACTIVATES FILLO TO INITIATE A FILL OPERATION, RIGHT ADJUSTING DATA IN THE ON-LINE BUFFER.

BCLK - BUFFER CLOCK

BCLK IS A FREE-RUNNING CLOCK WHICH DRIVES BUF SEQUENCERS AND WHICH IS BROUGHT OUT ON THE SERIAL BUFFER BUS FOR OPTIONAL USE BY DEVICES ON THIS BUS. BCLK IS A SQUARE WAVE PULSE TRAIN WITH A NOMINAL 600 NS PERIOD.

CTTC SHIFTING OF THE ON-LINE BUFFER IS SHOWN IN FIGURE 9 (SHT B3GF). THE TRAILING EDGE OF BACRO FIRES THE ON-LINE BUFFER COMPLETE MONOPULSER ØNLCMP, WHICH RAISES THE BR FLAG AND SWITCHES THE BUFFERS WITHOUT INTERFERING CTTC/BUF DATA TRANSFER. NOTE THAT IF THE BR FLAG IS STILL RAISED AT THE TRAILING EDGE OF ØNLCMP, AN OVERFLOW CONDITION EXISTS, THE BUFFERS DO NOT SWITCH, AND ON-LINE BUFFER CLOCKING IS INHIBITED.

3.4 ON-LINE SEQUENCER

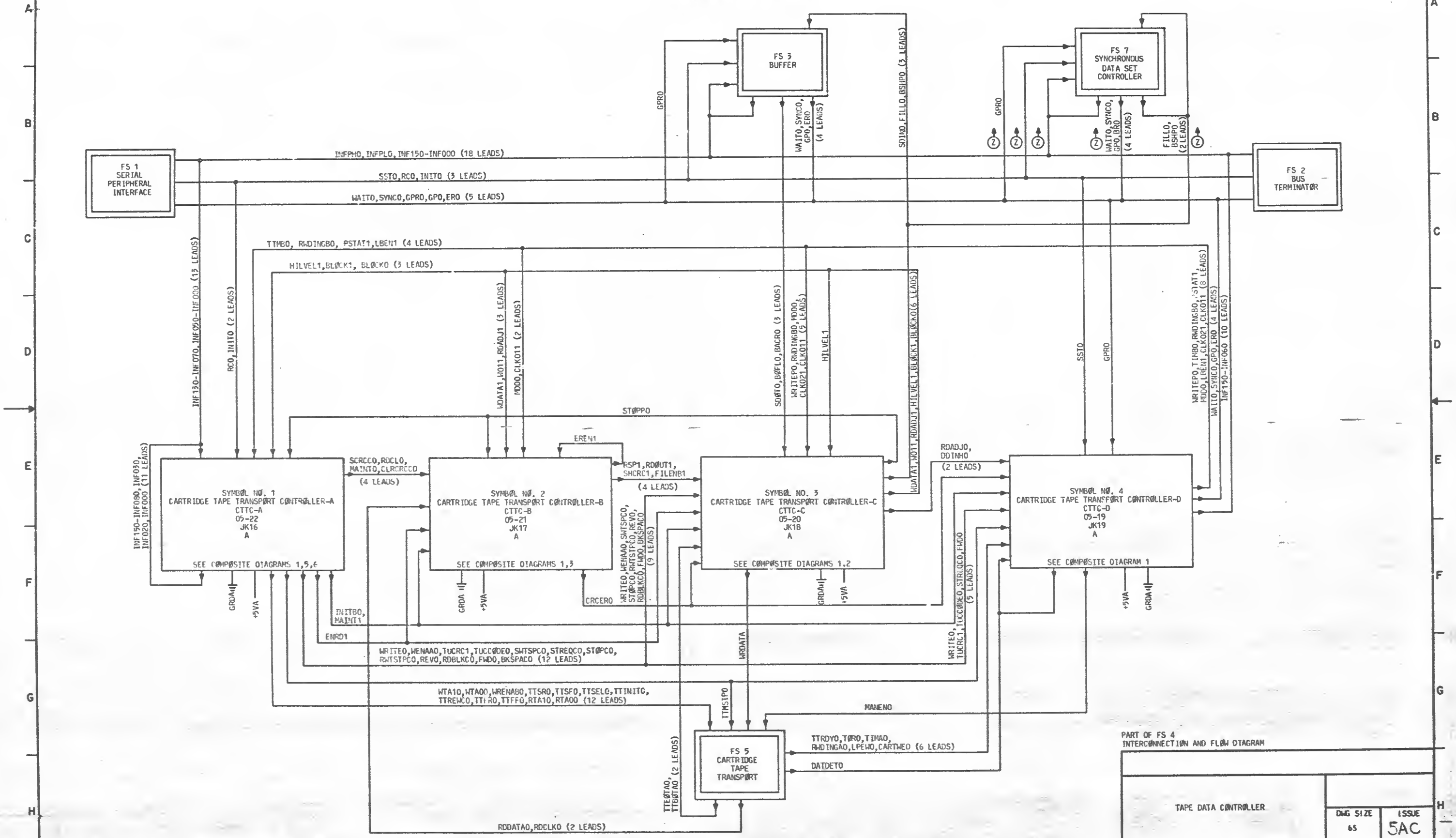
THE ON-LINE SEQUENCER ØNLSEQ HANDLES CTTC OR 3ACC REQUESTED FILL OPERATIONS. ØNLSEQ IS A THREE ELEMENT TIMING CHAIN (ØNLSEQA-C) DRIVEN BY BCLK. ACTION BEGINS WITH CTTC ASSERTION OF FILLO OR THE ACTIVATION OF THE COMMAND DECODER FILL OUTPUT, EITHER OF WHICH SET ØNLSEQA, FIGURE 10 (SHT B3GG). SUBSEQUENT NEGATIVE TRANSITIONS OF BCLK SET ELEMENTS ØNLSEQB AND C CONSECUTIVELY. ØNLSEQC ENABLES ON-LINE BUFFER SHIFTING BY A SERIES OF CLOCK PULSES DERIVED FROM BCLK. INFORMATION AT THE BUFFER OUTPUT WILL BE RECIRCULATED INTO THE BUFFER INPUT DURING A FILL OPERATION (NØRMALLY PADDING THE BUFFER WITH ZEROES) UNLESS THE CTTC HØLDS SDINO LØW, IN WHICH CASE THE BUFFER IS PADDED WITH ALL ØNES. THE TRAILING EDGE ØF BACRO INDICATES THE RIGHT ADJUSTMENT ØF THE ØN - LINE BUFFER IS CØMPLETE BY FIRING ØNLCMP, WHICH IN TURN RAISES THE BR FLAG AND SWITCHES BUFFERS. ØNLSEQ SUBSEQUENTLY DRØPS ØFF, TERMINATING FURTHER SHIFTING.

PART ØF FS 3
CØMPØSITE DIAGRAM 10

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B3GK

PART OF FS 4

CARTRIDGE TAPE TRANSPØRT CØNTRØLLER
INTERCØNNECTIØN AND FLØW DIAGRAM



PART OF FS 4
INTERCØNNECTIØN AND FLØW DIAGRAM

TAPE DATA CØNTRØLLER

DWG SIZE
6S

ISSUE
5AC

BELL LABORATORIES

SD-1C904-01

B4AA

E-7421 (12-73)

PRINTED IN U.S.A.

PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+5VA	+5 VOLT POWER BUS A
BACR0	SERIAL BUFFER BUS CARRY PULSE INDICATING THAT THE ON-LINE (ACTIVE) DATA BUFFER HAS BEEN EITHER FILLED OR EMPTIED, ACTIVE LOW
BKSPAC0	CTTC'S BACKSPACE COMMAND BEING DECODED, LOW ACTIVE
BLOCK0	STOP AFTER BLOCK, LOW ACTIVE
BLOCK1	STOP AFTER BLOCK, HIGH ACTIVE
BOFL0	SERIAL BUFFER BUS OVERFLOW INDICATION, ACTIVE LOW
BSHP0	SERIAL BUFFER BUS DATA SHIFT PULSE, ACTIVE LOW
CARTWE0	TAPE CARTRIDGE IS WRITE ENABLED STATUS LINE FROM CTT, ACTIVE LOW
CLK011	CTTC'S INTERNAL CLOCK PHASE ONE, ACTIVE HIGH
CLK021	CTTC'S INTERNAL CLOCK PHASE TWO, ACTIVE HIGH
CLRCRCC0	CTTC'S CLEAR THE CYLIC REDUNDANCY CHECK CIRCUIT COMMAND BEING DECODED, LOW ACTIVE
CRCER0	ERROR INDICATION OUTPUT OF THE CYCLIC REDUNDANCY CHECK CIRCUIT, ACTIVE LOW
DATDET0	DATA DETECT STATUS LINE FROM CTT, ACTIVE LOW
DDINH0	INHIBITS THE DATA DETECT STATUS SIGNAL FROM THE CTT UNTIL THE TAPE HAS ACCELERATED TO FULL SPEED DURING BACKSPACE, READ-A-BLOCK, AND READ-AFTER-WRITE OPERATIONS, ACTIVE LOW
ENRD1	ENABLE THE READ CIRCUITS OF THE CTTC TO ACCEPT READ DATA FROM THE CTT, ACTIVE HIGH
EREN1	CRCC ERROR OUTPUT ENABLE, ACTIVE HIGH
ER0	REQUEST TO THE SPI TO TRANSMIT AN ERROR START CODE IN THE CURRENT STATUS REPLY TO THE CC, LOW ACTIVE
FILENB1	CTTC'S FILL REQUEST CIRCUIT ENABLE, ACTIVE HIGH
FILL0	SERIAL BUFFER BUS FILL OPERATION REQUEST, ACTIVE LOW
FWD0	CTTC'S TAPE MOTION REQUEST REGISTER IS SET TO FAST OR SLOW FORWARD, ACTIVE LOW
GPR0	REPLY FROM BT TO ACKNOWLEDGE THE RECEIPT OF A GP0 REQUEST, LOW ACTIVE
GP0	REQUEST TO BT TO GENERATE PARITY OVER THE STATUS REPLY CURRENTLY RESIDING ON THE COMMON PARALLEL BUS
GRDA	GROUND RETURN FOR +5V POWER BUS A
HILVEL1	SOURCE OF A HIGH LOGIC LEVEL USED TO DISABLE UNUSED LOGIC INPUTS
INF(00-15)0	COMMON PARALLEL BUS BITS (00-15), LOW = LOGICAL ONE
INITB0	TDC INITIALIZE COMMAND EXECUTE (LOGICALLY EQUIVALENT TO INIT0), ACTIVE LOW
INIT0	TDC INITIALIZE COMMAND, LOW ACTIVE
LBEN1	ENABLE PARALLEL LOADING OF THE INFORMATION BUS, HIGH ACTIVE
LPEW0	STATUS PULSE FROM CTT TO INDICATE THAT THE CTT HAS SENSED THE LOAD POINT OR EARLY WARNING HOLE MARK ON THE TAPE, ACTIVE LOW
MAINT0	CTTC IS IN THE MAINTENANCE MODE OF OPERATION, ACTIVE LOW
MAINT1	CTTC IS IN THE MAINTENANCE MODE OF OPERATION, (COMPLEMENT OF MAINT0) ACTIVE HIGH
MANEN0	REQUEST TO THE CTT TO ENABLE THE OPERATORS REWIND AND UNLOAD MANUAL PUSH BUTTONS
MOD0	MODIFIED DATA DETECT STATUS FROM THE CTT, ACTIVE LOW
PSTAT1	GATE THE CTTC'S PRIMARY STATUS REPLY TO THE PARALLEL INFORMATION BUS, HIGH ACTIVE
RC0	RECEIVE THE DATA ON THE COMMON PARALLEL BUS AND INTERPRET IT AS A COMMAND, LOW ACTIVE
RDADJ0	READ DATA ADJUST FOR PROPER 16-BIT WORD FRAMING (COMPLEMENT OF RDADJ1), ACTIVE LOW
RDADJ1	READ DATA ADJUST FOR PROPER 16-BIT WORD FRAMING (COMPLEMENT OF RDADJ0), ACTIVE HIGH
RDBLKC0	CTTC'S READ-A-BLOCK COMMAND BEING DECODED, ACTIVE LOW
RDCLK0	READ DATA CLOCK FROM THE CTT, ACTIVE LOW
RDCL0	CLEAR THE CRC CHECK CIRCUIT FOR A READ OR READ-AFTER-WRITE OPERATION, ACTIVE LOW
RDDATA0	READ DATA FROM THE CTT, LOW = LOGICAL ONE
RDOUT1	READ DATA OUTPUT FROM DATA RECOVERY CIRCUITRY, LOGICAL ONE = HIGH
REV0	CTTC'S TAPE MOTION REQUEST REGISTER IS SET TO FAST OR SLOW REVERSE, ACTIVE LOW
RSP1	READ SHIFT PULSE USED TO GENERATE DATA SHIFT PULSES TO THE BUFFER, ACTIVE HIGH
RTA00	READ TRACK SELECTOR ADDRESS BIT ZERO (LSB), LOW = LOGICAL ONE
RTA10	READ TRACK SELECTOR ADDRESS BIT ONE (MSB), LOW = LOGICAL ONE
RWDINGA0	CTT IS PERFORMING A TAPE REWIND SEQUENCE (LOGICALLY EQUIVALENT TO RWDINGB0), LOW ACTIVE
RWDINGB0	CTT IS PERFORMING A TAPE REWIND SEQUENCE (LOGICALLY EQUIVALENT TO RWDINGA0), LOW ACTIVE
RWTSTPC0	CTTC'S RESET WRITE STOP CIRCUIT COMMAND BEING DECODED, LOW ACTIVE
SCRCC0	CTTC'S SHIFT CYCLIC REDUNDANCY CHECK CIRCUIT COMMAND BEING DECODED, LOW ACTIVE
SDIN0	SERIAL BUFFER BUS DATA INPUT TO THE BUFFER UNIT, LOW = LOGICAL ONE
SDOT0	SERIAL BUFFER BUS DATA OUTPUT FROM THE BUFFER UNIT, LOW = LOGICAL ONE
SHCRC1	CYCLIC REDUNDANCY CHECK CIRCUIT DATA SHIFT CLOCK, ACTIVE HIGH
SST0	ADDRESSED DEVICE REQUESTED TO GATE A STATUS REPLY ON THE COMMON PARALLEL BUS, ACTIVE LOW
STOPC0	CTTC'S STOP COMMAND BEING DECODED, ACTIVE LOW
STOPP0	TAPE IS STOPPING DELAY TIMING PULSE, LOW ACTIVE
STREQC0	CTTC'S SECONDARY STATUS REQUEST COMMAND BEING DECODED, ACTIVE LOW
SWTSTPC0	CTTC'S SET WRITE STOP COMMAND BEING DECODED, ACTIVE LOW
SYNC0	A SYNCHRONIZING SIGNAL TO THE SPI WHICH INDICATES THAT A DEVICE HAS SENSED A COMMAND ON THE PARALLEL BUS, ACTIVE LOW
TIMA0	TAPE IS MOVING STATUS BIT FROM CTT (LOGICALLY EQUIVALENT TO TIMB0), ACTIVE LOW
TIMB0	TAPE IS MOVING STATUS BIT FROM CTT (LOGICALLY EQUIVALENT TO TIMA0), ACTIVE LOW
TOR0	TAPE OFF REEL STATUS LINE FROM CTT, ACTIVE LOW
TTBOTA0	PHYSICAL BEGINNING OF TAPE STATUS LINE FROM CTT, ACTIVE LOW
TTEOTA0	PHYSICAL END-OF-TAPE STATUS BIT FROM CTT (LOGICALLY EQUIVALENT TO TTEOTB0), ACTIVE LOW
TTFF0	FAST (90 IPS) FORWARD TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TTFR0	FAST (90 IPS) REVERSE TAPE MOTION REQUEST TO THE CTT, ACTIVE LOW
TTINIT0	TRANSPORT INITIALIZE REQUEST LINE TO THE CTT, ACTIVE LOW
TTMSTP0	TRANSPORT MAINTENANCE STOP REQUEST LINE TO THE CTT, ACTIVE LOW
TTRDY0	CTT READY STATUS BIT FROM CTT, LOW ACTIVE
TTREWC0	TAPE REWIND REQUEST LINE TO THE CTT, ACTIVE LOW
TTSEL0	TRANSPORT SELECT LINE TO THE CTT, ACTIVE LOW
TTSF0	SLOW (30 IPS) FORWARD TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TTSR0	SLOW (30 IPS) REVERSE TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TUCCODE0	CTTC'S 3-OUT-OF-6 DEVICE SELECTIONS CODE IS PRESENT ON THE PARALLEL INFORMATION BUS LINES INF000 THROUGH INF050 DURING RC0, ACTIVE LOW
TUCRC1	SPI'S, RECEIVE COMMAND SIGNAL, BUFFERED FOR USE BY THE CTTC (LOGICALLY THE COMPLEMENT OF RC0), ACTIVE HIGH
WAIT0	A REQUEST TO THE SPI TO WAIT UNTIL THE DEVICE HAS HAD TIME TO ACT UPON A COMMAND BEFORE REMOVING THAT COMMAND FROM THE PARALLEL BUS, ACTIVE LOW
WDATA1	WRITE DATA BEING PRESENTED TO THE CTTC'S PHASE ENCODING CIRCUITRY, HIGH = LOGICAL ONE
WENAA0	OUTPUT OF THE CTTC'S WRITE CIRCUITRY ENABLE FLIP-FLOP (LOGICALLY EQUIVALENT TO WRENAB0), ACTIVE LOW
WRDATA	PHASE ENCODED WRITE DATA OUTPUT TO THE CTT
WRENAB0	WRITE CIRCUITRY ENABLE REQUEST LINE TO THE CTT (LOGICALLY EQUIVALENT TO WENAA0), ACTIVE LOW
WRITEP0	WRITE DATA DELAY PULSE USED TO DELAY THE STARTING OF THE WRITE DATA OPERATION UNTIL THE TAPE IS MOVING AT FULL SPEED AND THE PROPER LENGTH IBG HAS BEEN WRITTEN, ACTIVE LOW
WRITE0	CTTC'S WRITE-A-BLOCK COMMAND IS BEING DECODED AND A NONWRITE PROTECTED TRACK IS SELECTED, ACTIVE LOW
WTA00	WRITE TRACK SELECTOR ADDRESS BIT ZERO (LSB), LOW = LOGICAL ONE
WTA10	WRITE TRACK SELECTOR ADDRESS BIT ONE (MSB), LOW = LOGICAL ONE
W011	CTTC'S WRITE CLOCK PHASE ONE, ACTIVE HIGH

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

B4AB

PRINTED IN U. S. A.

06/15/77

PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

SYMBOL NO. 1

CARTRIDGE TAPE TRANSPORT CONTROLLER - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-A	05-22	JK16	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		003			WENAB1	2H2
		004			ENRDO	2H0
		005			WTBG	2H8
		006			MOTCINH1	2H3
		011			READCO	2H5
		013			TTFF1	2H3
		014			TTSF1	2H1
		105			WETRK10	2A9
		107			WRCKTENO	2H1
		108			TTFR1	2H3
		112			FSTREVCO	2H5
		118			TTSR1	2H3
		210			FSTFORCO	2H5
		300			TRCKA01	3H5
		303			TRCKA11	3H5
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
BKSPACO	O	110	4/3		BKSPACO	2H5
BLOCKO	I	009	4/3		BLOCKO	3A2
BLOCK1	I	318	4/3		BLOCK1	3A1
CLRCRCCO	O	311	4/2		CLRCRCCO	2H6
ENRO1	O	114	4/2,4/3		ENRD1	2H0
FWDO	OI	207	4/3,4/4		FWDO	2H3
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
HILVEL1	I	008	4/3		IBGSTPO	3A3
INF000	OI	201	1/1		INF000	3A8
INF010	I	101	1/1		INF010	2A1
INF020	OI	202	1/1		INF020	3A8
INF030	OI	302	1/1		INF030	3A8
INF040	I	002	1/1		INF040	2A1
INF050	I	102	1/1		INF050	2A1
INF070	I	308	1/1		INF070	2A7
INF080	OI	217	1/1		INF080	3A4
INF090	OI	212	1/1		INF090	2A5
INF100	OI	213	1/1		INF100	2A6
INF110	OI	214	1/1		INF110	2A6
INF120	OI	115	1/1		INF120	3A5
INF130	OI	015	1/1		INF130	3A6
INF140	OT	203	1/1		INF140	3H4
INF150	OT	204	1/1		INF150	3H1
INITBO	OI	205	4/2,4/3 4/4		INITBO	2H7
INITO	I	219	1/3		INITO	2A7
LBEN1	I	304	4/4		LBEN1	3A7
MAINTO	OI	007	4/2		MAINTO	3H7
MAINT1	O	305	4/2,4/3 4/4		MAINT1	3H7
PSTAT1	I	001	4/4		PSTAT1	3A0
RCO	I	103	1/3		RCO	2A0
RDBLKCO	OI	010	4/3		RDBLKCO	2H5
RDCLO	O	215	4/2		RDCLO	2H0
REVO	O	208	4/3		REVO	2H2
RTA00	O	117	5/2		RTA00	3H5
RTA10	O	317	5/2		RTA10	3H6
RWDINGBO	I	019	4/4		RWDINGBO	3A3
RWTSTPCO	O	313	4/3		RWTSTPCO	2H6

SYMBOL NO. 1 (CONT)

CARTRIDGE TAPE TRANSPORT CONTROLLER - A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-A	05-22	JK16	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
SCRCCO	O	312	4/2		SCRCCO	2H6
STOPCO	O	012	4/3		STOPCO	2H6
STOPPO	I	113	4/3		STOPPO	2A0
STREQCO	O	310	4/4		STREQCO	2H6
SWTSTPCO	O	314	4/3		SWTSTPCO	2H6
TIMBO	I	106	4/4		TIMBO	2A3
TTFFO	O	216	5/1		TTFFO	2H4
TTFRO	O	016	5/1		TTFRO	2H5
TTINITO	O	209	5/1		TTINITO	2H8
TTMSTPO	O	309	4/4,5/1.		TTMSTPO	2H6
TTREWCO	O	111	5/1		TTREWCO	2H6
TTSELO	O	315	5/1		TTSELO	3H7
TTSFO	O	116	5/1		TTSFO	2H4
TTSRO	O	316	5/1		TTSRO	2H4
TUCCODEO	O	211	4/4		TUCCODEO	2H0
TUCRC1	OI	301	4/4		TUCRC1	2H0
WENAAO	OI	109	4/3		WENAAO	2H1
WRENABO	OT	100	5/2		WRENABO	2H2
WRITEO	OI	104	4/3,4/4		WRITEO	2H8
WTA00	O	218	5/2		WTA00	3H5
WTA10	O	017	5/2		WTA10	3H6

SYMBOL NO. 2

CARTRIDGE TAPE TRANSPORT CONTROLLER - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-B	05-21	JK17	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		009			RSTPO	3H4
		107			RDDATA	2H0
		108			RSTPN1	3H6
		112			ERDET1	2H6
		115			RDDATA1	3H6
		202			MDDNP1	3H6
		300			HILEV1	3A3
		301			RDCLKPO	3H7
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
CLK011	I	114	4/4		CLK011	3A0
CLRCRCCO	I	206	4/1		CLRCRCCO	2A2
CRCERO	O	113	4/3,4/4		CRCERO	2H7
ENRO1	I	013	4/1		ENRD1	3A1
EREN1	O	003			ERENOUT1	3H6
	I	014			ERENIN1	2A9
..LENB1	O	201	4/3		FILENB1	3H8
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INITBO	I	210	4/1		INITBO	2A4
MAINTO	I	305	4/1		MAINTO	2A3
MAINT1	I	207	4/1		MAINT1	2A2

SYMBOL NO. 2 (CONT)

CARTRIDGE TAPE TRANSPORT CONTROLLER - B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-B	05-21	JK17	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
MDDO	I	015	4/4		MDDO	3A8
RDADJ1	I	115	4/3		RDADJ1	3A0
RDCLKO	I	218	5/2		RDCLKO	3A7
RDCLO	I	306	4/1		RDCLO	2A2
RDDATAO	I	318	5/2		RDDATAO	3A2
RDOUT1	O	002	4/3		RDOUT1	2H5
RSP1	OI	017	4/3		RSP1	3H4
SCRCCO	I	103	4/1		SCRCCO	2A3
SHCRC1	O	102	4/3		SHCRC1	3H5
STOPPO	I	008	4/3		STOPPO	2A1
WDATA1	I	116	4/3		WDATA1	3A2
WO11	I	316	4/3		WO11	3A1

SYMBOL NO. 3

CARTRIDGE TAPE TRANSPORT CONTROLLER - C

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-C	05-20	JK18	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		209			STOPPAO	3H4
		303			FILLAO	3H6
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
BACRO	I	315	3/4		BACRO	3A2
BKSPACO	I	017	4/1		BKSPACO	4A6
BLOCKO	O	001	4/1		BLOCKO	4H6
BLOCK1	O	201	4/1		BLOCK1	4H5
BOFLO	I	317	3/2		BOFLO	4A0
BSHPO	OT I	006	(Z)7/2 2/1,3/2		BSHPO	2H4
CLK011	I	018	4/4		CLK011	2A1
CLK021	I	118	4/4		CLK021	2A0
CRCERO	I	300	4/2		CRCERO	4A0
DDINHO	O	002	4/4		DDINHO	4H6
ENRD1	I	207	4/1		ENRD1	3A6
FILENB1	I	003	4/2		FILENB1	3A6
FILLO	OT I	004	(Z)7/2 2/1,3/2		FILLO	3H5
FWDO	I	316	4/1		FWDO	4A1
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
HILVEL1	OI	218	4/1		HILVEL1	3H2
	I	104	4/3		HILVL1	4A0
INITBO	I	009	4/1		INITBO	4A0
MAINT1	I	108	4/1		MAINT1	4A3
MDDO	I	103	4/4		MDDO	4A5
RDADJO	O	310	4/4		RDADJO	2H9
RDADJ1	OI	109	4/2		RDADJ1	2H7
RDBLKCO	I	016	4/1		RDBLKCO	4A6

SYMBOL NO. 3 (CONT)

CARTRIDGE TAPE TRANSPORT CONTROLLER - C

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-C	05-20	JK18	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
RDOUT1	I	208	4/2		RDOUT1	3A6
REVO	I	219	4/1		REVO	4A1
RSP1	I	101	4/2		RSP1	2A4
RWDINGBO	I	013	4/4		RWDINGBO	4A5
RWTSTPCO	I	117	4/1		RWTSTPCO	3A3
SDINO	OT	306	3/2		SDINO	3H6
SDOTO	I	214	3/4		SDOTO	2A5
SHCRC1	I	106	4/2		SHCRC1	3A5
STOPCO	I	012	4/1		STOPCO	4A3
STOPPO	O	301	4/1,4/2		STOPPO	4H3
SWTSTPCO	I	318	4/1		SWTST	3A3
TTBOTAO	I	302	5/1		TTBOTO	4A2
TTEOTAO	I	113	5/1		TTEOTAO	4A2
WDATA1	OI	102	4/2		WDATA1	2H4
WENAAO	I	107	4/1		WENAAO	3A5
WRDATA	O	312	5/2		WRDATA	2H3
WRITEPO	I	019	4/4		WRITEPO	2A0
WRITEO	I	211	4/1		WRITEO	4A6
WO11	OI	010	4/2		WO11	2H1

PART OF FS 4
SYMBOL(S) 1 2 3

TAPE DATA CONTROLLER

DWG SIZE	ISSUE
C2	5AC

BELL LABORATORIES
SD-1C904-01
B4CA
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PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

SYMBOL NO. 4

CARTRIDGE TAPE TRANSPORT CONTROLLER - D

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTTC-D	05-19	JK19	A	

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		001			LPEW1	3H2
		007			RDY0	2H2
		107			BOTSTAT1	3H3
		111			EOTSTAT1	3H3
		302			TTRDY1	2H4
		312			SSTAT1	2H1
+5VA	PWR	000		203	+5V	
	PWR	119		203	+5V	
CARTWE0	I	201	5/1		CARTWE0	2A3
CLK011	O	011	4/2,4/3		CLK011	2H5
CLK021	O	016	4/3		CLK021	2H6
CRCER0	I	114	4/2		CRCER0	2A2
DATDET0	I	219	5/2		DATDET0	3A8
DDINH0	I	014	4/3		DDINH0	3A8
ER0	OT	006	2/1		ER0	2H2
FWD0	I	008	4/1		FWD0	3A3
GPR0	I	103	2/1		GPR0	2A3
GP0	OT	303	3/1		GP0	2H4
GRDA	GRD	0GD		203	GRD	
	GRD	2GD		203	GRD	
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INF060	OI	304	1/1		INF060	2H3
INF070	OI	203	1/1		INF070	2H4
INF080	OT	214	1/1		INF080	3H4
INF090	OT	315	1/1		INF090	3H7
INF100	OT	317	1/1		INF100	3H7
INF110	OT	017	1/1		INF110	3H8
INF120	OT	217	1/1		INF120	3H9
INF130	OT	218	1/1		INF130	3H1
INF140	OT	013	1/1		INF140	3H3
INF150	OT	012	1/1		INF150	3H0
INITB0	I	112	4/1		INITB0	2A2
LBEN1	O	101	4/1		LBEN1	2H2
LPEW0	I	300	5/1		LPEW0	3A2
MAINT1	I	316	4/1		MAINT1	3A9
MANEN0	O	009	5/1		MANEN0	3H0
MOD0	O	113	4/2,4/3		MOD0	3H8
PSTAT1	O	106	4/1		PSTAT1	2H1
RDADJ0	I	205	4/3		RDADJ0	3A9
RWDINGA0	I	019	5/1		RWDINGA0	3A2
RWDINGB0	O	010	4/1,4/3		RWDINGB0	3H2
SST0	I	117	1/3		SST0	2A0
STREDC0	I	105	4/1		STPEDC0	2A0
SYNC0	OT	306	2/1		SYNC0	2H0
TIMA0	I	118	5/1		TIMA0	3A7
TIMB0	O	115	4/1		TIMB0	3H8
TOR0	I	018	5/1		TOR0	3A6
TTMSTP0	I	216	4/1		TTMSTP0	2A0
TTRDY0	I	301	5/1		TTRDY0	2A4
TUCCODE0	I	206	4/1		TUCCODE0	2A1
TUCRC1	I	015	4/1		TUCRC1	2A1
WAIT0	OT	100	2/1		WAIT0	2H3
WRITEP0	O	109	4/3		WRITEP0	4H3
WRITE0	I	110	4/1		WRITE0	4A0

PART OF FS 4
SYMBOL(S) 4

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

B4CB

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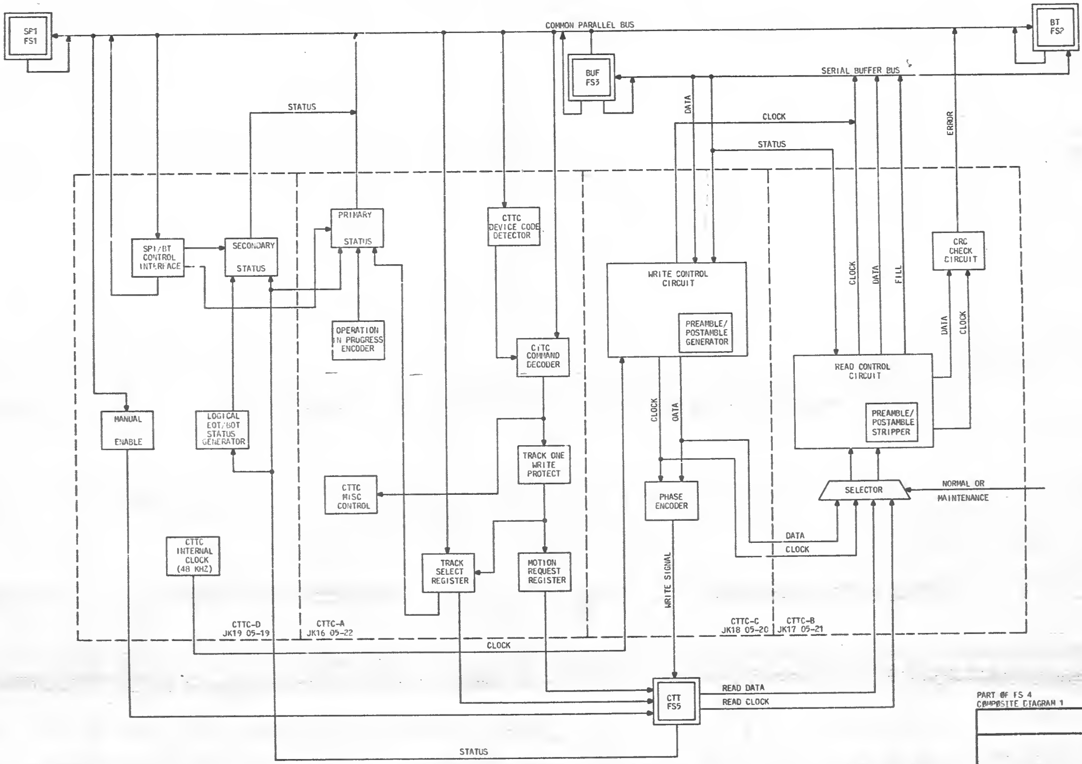
PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM I

FUNCTIONAL BLOCK DIAGRAM OF
CARTRIDGE TAPE TRANSPORT CONTROLLER



PART OF FS 4
COMPOSITE DIAGRAM 1

TAPE DATA CONTROLLER ②	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B4GA

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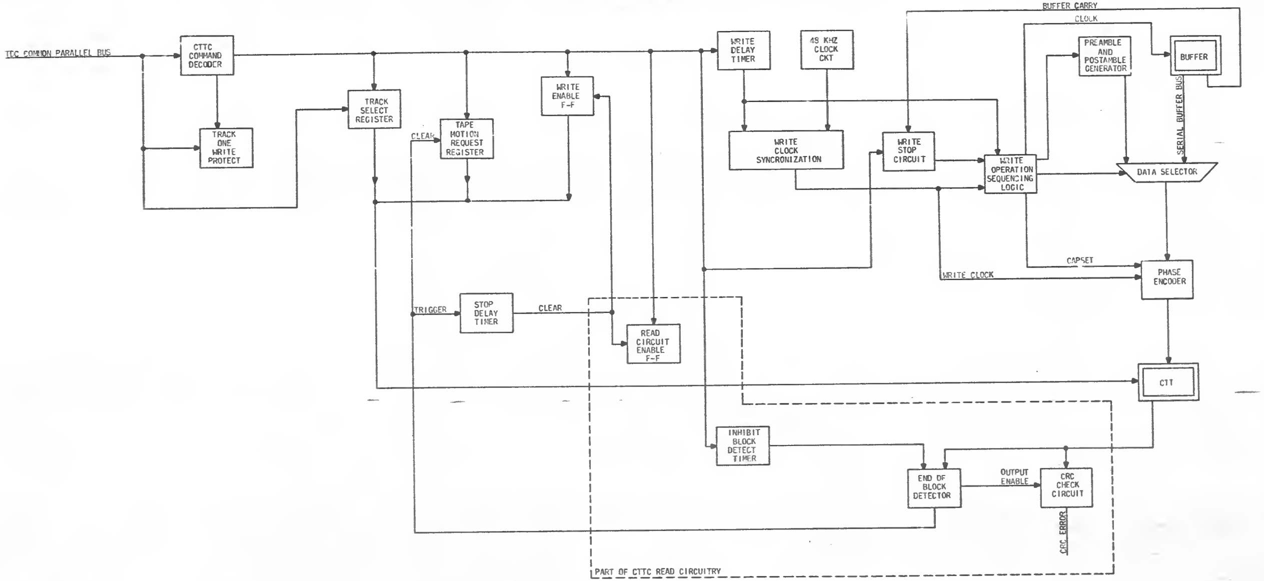
CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM 2

CTTC-WRITE CIRCUITRY FUNCTIONAL BLOCK DIAGRAM



PART ØF FS 4
CØMPØSITE DIAGRAM 2

TAPE DATA CONTROLLER ②	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-1C904-01	B4GB

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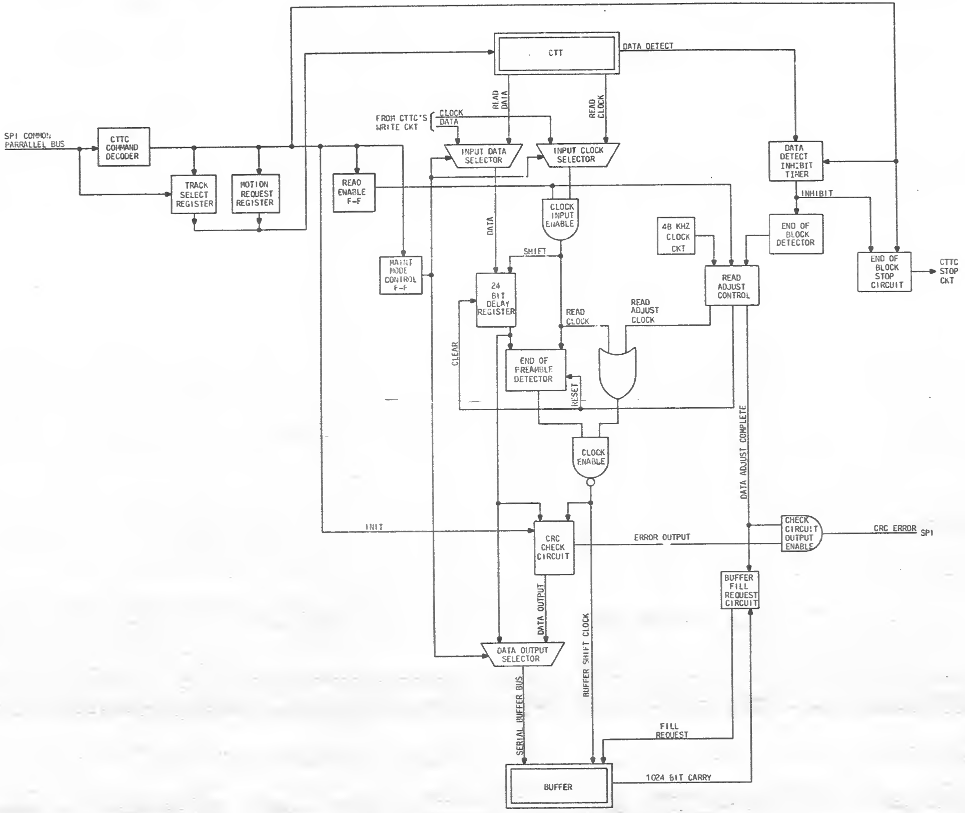
CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM 3

CTTC-READ CIRCUIT FUNCTIONAL BLOCK DIAGRAM



PART ØF FS 4
CØMPØSITE DIAGRAM 3

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 2A
BELL LABORATORIES	SD-IC904-01	B4GC

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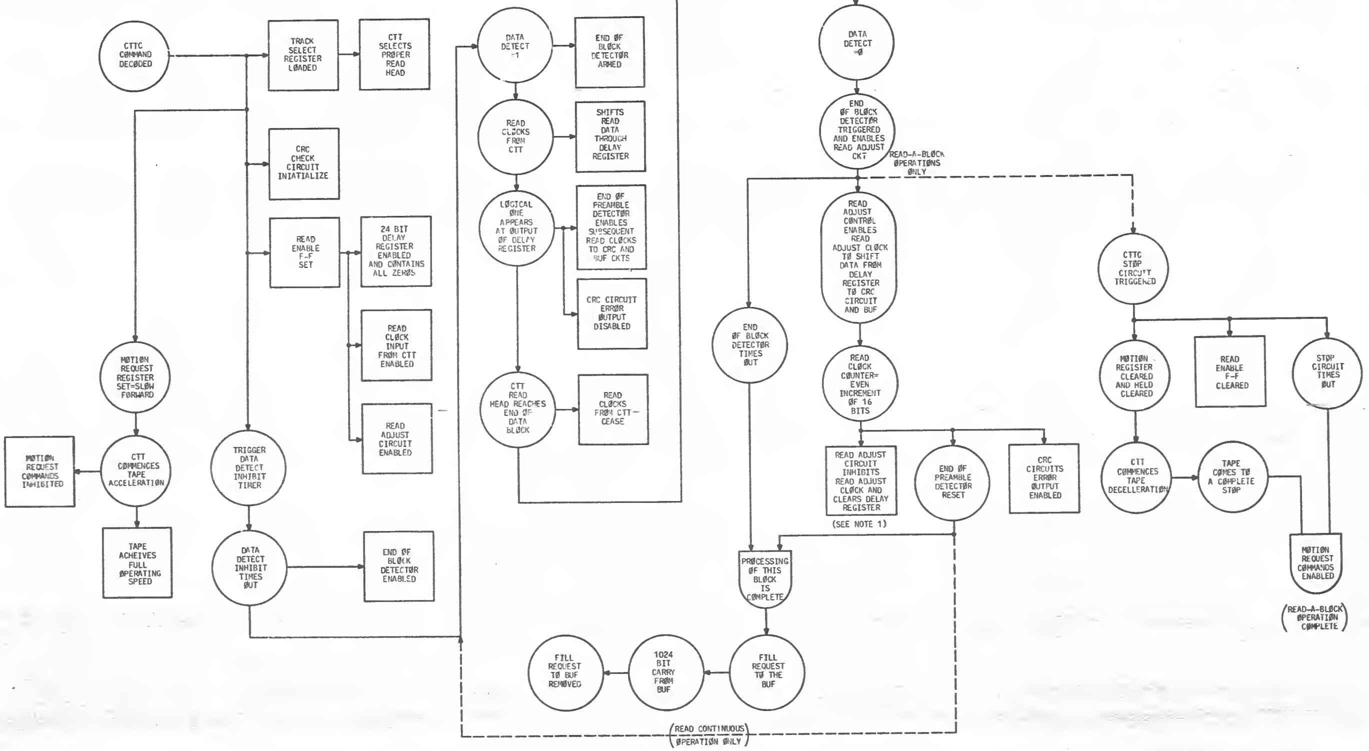
CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM 4

CTTC-READ AND READ-A-BLOCK SEQUENCE DIAGRAM

NOTES:

1. DATA POSTAMBLE IS STRIPPED BY BEING LEFT IN THE DELAY REGISTER AT THE TERMINATION OF A READ ADJUST OPERATION.



CTTC COMMAND DECODED
TRACK SELECT REGISTER LOADED
CTT SELECTS PROPER READ HEAD
CRC CHECK CIRCUIT INIATIALIZE
READ ENABLE F-F SET
24 BIT DELAY REGISTER ENABLED AND CONTAINS ALL ZEROS
READ CLOCK INPUT FROM CTT ENABLED
READ ADJUST CIRCUIT ENABLED
MOTION REQUEST REGISTER SET=SLOW FORWARD
CTT COMMENCES TAPE ACCELERATION
MOTION REQUEST COMMANDS INHIBITED
TAPE ACHEIVES FULL OPERATING SPEED
TRIGGER DATA DETECT INHIBIT TIMER
DATA DETECT INHIBIT TIMES OUT
END OF BLOCK DETECTOR ENABLED
DATA DETECT =1
END OF BLOCK DETECTOR ARMED
READ CLOCKS FROM CTT
SHIFTS READ DATA THROUGH DELAY REGISTER
LOGICAL ONE APPEARS AT OUTPUT OF DELAY REGISTER
END OF PREAMBLE DETECTOR ENABLES SUBSEQUENT READ CLOCKS TO CRC AND BUF CKTS
CRC CIRCUIT ERROR OUTPUT DISABLED
CTT READ HEAD REACHES END OF DATA BLOCK
READ CLOCKS FROM CTT CEASE
DATA DETECT =0
END OF BLOCK DETECTOR TRIGGERED AND ENABLES READ ADJUST CKT
READ-A-BLOCK OPERATIONS ONLY
READ ADJUST CONTROL ENABLES READ ADJUST CLOCK TO SHIFT DATA FROM DELAY REGISTER TO CRC CIRCUIT AND BUF
END OF BLOCK DETECTOR TIMES OUT
READ CLOCK COUNTER= EVEN INCREMENT OF 16 BITS
READ ADJUST CIRCUIT INHIBITS READ ADJUST CLOCK AND CLEARS DELAY REGISTER
(SEE NOTE 1)
END OF PREAMBLE DETECTOR RESET
CRC CIRCUITS ERROR OUTPUT ENABLED
PROCESSING OF THIS BLOCK IS COMPLETE
FILL REQUEST TO THE BUF
1024 BIT CARRY FROM BUF
FILL REQUEST TO BUF REMOVED
(READ CONTINUOUS OPERATION ONLY)
CTTC STOP CIRCUIT TRIGGERED
MOTION REGISTER CLEARED AND HELD CLEARED
READ ENABLE F-F CLEARED
STOP CIRCUIT TIMES OUT
CTT COMMENCES TAPE DECELLERATION
TAPE COMES TO A COMPLETE STOP
MOTION REQUEST COMMANDS ENABLED
(READ-A-BLOCK OPERATION COMPLETE)

PART OF FS 4
COMPOSITE DIAGRAM 4

TAPE DATA CONTROLLER

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

SD-1C904-01-B4GD

ISSUE
2A

PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM 5

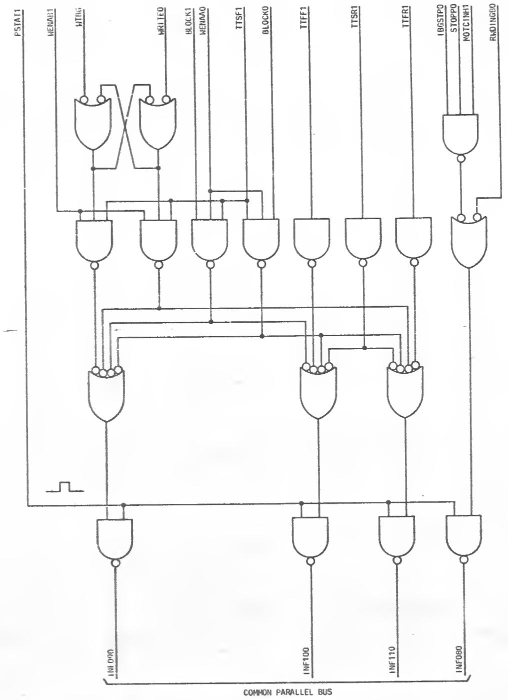
CTTC – OPERATION IN PROGRESS ENCODER

OPERATION IN PROGRESS	OPERATION CODE				CIRCUIT INPUTS													
	INF110	INF100	INF090	INF080	WENAB1	WWIBG1	WWIBG1	BLOCK1	WENAA0	TTSF1	BLOCK0	TTFF1	TTSR1	TTFR1	IBGSTP0	STOPP0	MOTCINH1	RWDING90
STOPPED OR STOPPING	0	0	0	0						L		L	L	L		L	L	H
REWINDING	0	0	0	1						L		L	L	L				L
WRITE CONTINUOUS IBG	0	0	1	1	H	H	L		L	H		L	L	L	H	H	H	
FAST FORWARD	0	1	0	1						L		H	L	L	H	H	H	
READ-A-BLOCK	0	1	1	1	L			H	H	H	L		L	L	H	H	H	
FAST REVERSE	1	0	0	1						L		L	L	H	H	H	H	
WRITE	1	0	1	1	H		H		L	H		L	L		H	H	H	
BACKSPACE	1	1	0	1						L			H		H	H	H	
READ CONTINUOUS	1	1	1	1					H	H	H				H	H	H	

L – LOW LOGIC LEVEL

H – HIGH LOGIC LEVEL

ALL OTHER – IRRELEVANT



PART OF FS 4
COMPOSITE DIAGRAM 5

TAPE DATA CONTROLLER ②		DWG SIZE 65	ISSUE 2A
BELL LABORATORIES	SD-1C904-01		B4GE

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E-702* (12-73)

PART OF FS 4

CARTRIDGE TAPE TRANSPORT CONTROLLER

COMPOSITE DIAGRAM 6

LOGICAL EOT AND BOT STATUS GENERATION

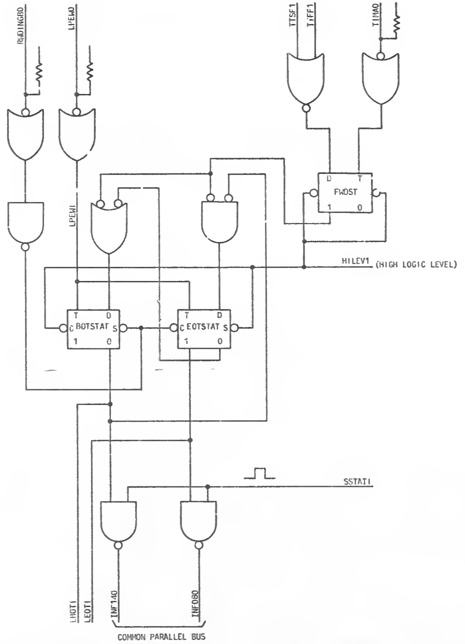
LOGICAL EOT STATUS GENERATION

LPEWO	BOT STATUS	FWDST	RWDINGAO	LOGICAL END OF TAPE STATUS
↘	0	1	0	1
	0	0		0
	1	1		0
	1	0		0
X	X	X	1	0

LOGICAL BOT STATUS GENERATION

LPEWO	EOT STATUS	FWDST	RWDINGAO	LOGICAL BEGINING OF TAPE STATUS
↘	0	1	0	0
	0	1		0
	1	1		0
	1	0		1
X	X	X	1	0

0	LOGICAL ZERO OR NOT ASSERTED
1=	LOGICAL ONE OR ASSERTED
X	IRRELEVANT
↘	HIGH TO LOW LOGIC TRANSITION



PART ØF FS 4
CØMPØSITE DIAGRAM 6

TAPE DATA CONTROLLER

②

DWG SIZE 6S

ISSUE 5AC

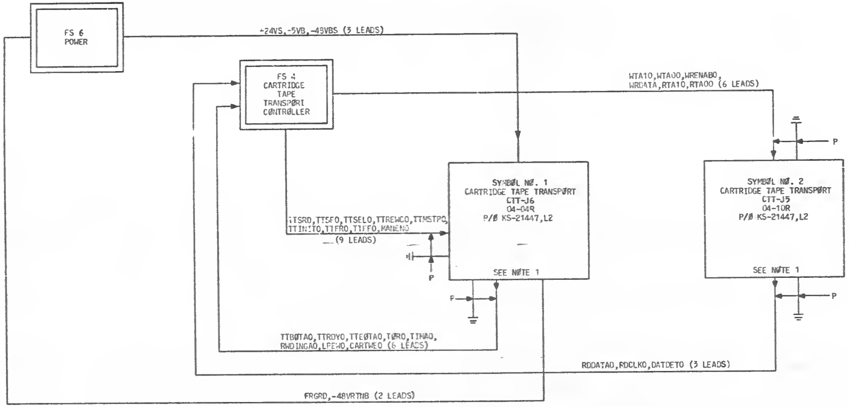
BELL LABORATORIES | SD-1C904-01 | B4GF

PART OF FS 5

CARTRIDGE TAPE TRANSPORT
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. LEADS INDICATED SHALL BE PAIRED AND TWISTED WITH A SIMILARLY NAMED GROUND LEAD RUNNING FROM THE CARTRIDGE TAPE TRANSPORT TO AN INTERMEDIATE CTF STAGING AREA.



PART OF FS 5
INTERCONNECTION AND FLOW DIAGRAM

TAPE DATA CONTROLLER

(2)

DWG SIZE
6S

ISSUE
2A

BELL LABORATORIES

SD-1C904-01

B5AA

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PART OF FS 5

CARTRIDGE TAPE TRANSPORT

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+24VS	+24 VOLT POWER BUS FROM THE TDC POWER SWITCH
+5VB	+5 VOLT POWER BUS B
-48VBS	-48 VOLT POWER BUS FROM TDC POWER SWITCH TO CTT (SUPPLIED FROM -48VB)
-48VRTNB	-48 VOLT POWER BUS B GROUND RETURN FROM CTT
CARTWEO	TAPE CARTRIDGE IS WRITE ENABLED STATUS LINE FROM CTT, ACTIVE LOW
CARTWEOG	GROUND LEAD TWISTED WITH CARTWEO
DATDETO	DATA DETECT STATUS LINE FROM CTT, ACTIVE LOW
DATDETOG	GROUND LEAD TWISTED WITH DATDETO
FRGRD	FRAME GROUND
LPEWO	STATUS PULSE FROM CTT TO INDICATE THAT THE CTT HAS SENSED THE LOAD POINT OR EARLY WARNING HOLE MARK ON THE TAPE, ACTIVE LOW
LPEWOG	GROUND LEAD TWISTED WITH LPEWO
MANENO	REQUEST TO THE CTT TO ENABLE THE OPERATORS REWIND AND UNLOAD MANUAL PUSH BUTTONS
MANENOG	GROUND LEAD TWISTED WITH MANENO
RDCLKO	READ DATA CLOCK FROM THE CTT, ACTIVE LOW
RDCLKOG	GROUND LEAD TWISTED WITH RDCLKO
RDDATAO	READ DATA FROM THE CTT, LOW = LOGICAL ONE
RDDATAOG	GROUND LEAD TWISTED WITH RDDATAO
RTA00	READ TRACK SELECTOR ADDRESS BIT ZERO (LSB), LOW = LOGICAL ONE
RTA00G	GROUND LEAD TWISTED WITH RTA00
RTA10	READ TRACK SELECTOR ADDRESS BIT ONE (MSB), LOW = LOGICAL ONE
RTA10G	GROUND LEAD TWISTED WITH RTATO
RWDINGAO	CTT IS PERFORMING A TAPE REWIND SEQUENCE (LOGICALLY EQUIVALENT TO RWDINGBO), LOW ACTIVE
RWDINGOG	GROUND LEAD TWISTED WITH RWDINGAO
TIMAO	TAPE IS MOVING STATUS BIT FROM CTT (LOGICALLY EQUIVALENT TO TIMBO), ACTIVE LOW
TIMAOG	GROUND LEAD TWISTED WITH TIMAO
TORO	TAPE OFF REEL STATUS LINE FROM CTT, ACTIVE LOW
TOROG	GROUND LEAD TWISTED WITH TORO
TTEOTAO	PHYSICAL END-OF-TAPE STATUS BIT FROM CTT (LOGICALLY EQUIVALENT TO TTEOTBO), ACTIVE LOW
TTEOTAOG	GROUND LEAD TWISTED WITH TTEOTAO
TTFFO	FAST (90 IPS) FORWARD TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TTFFOG	GROUND LEAD TWISTED WITH TTFFO
TTFRO	FAST (90 IPS) REVERSE TAPE MOTION REQUEST TO THE CTT, ACTIVE LOW

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
TTFROG	GROUND LEAD TWISTED WITH TTFRO
TTINITO	TRANSPORT INITIALIZE REQUEST LINE TO THE CTT, ACTIVE LOW
TTINITOG	GROUND LEAD TWISTED WITH TTINITO
TTMSTPO	TRANSPORT MAINTENANCE STOP REQUEST LINE TO THE CTT, ACTIVE LOW
TTMSTPOG	GROUND LEAD TWISTED WITH TTMSTPO
TTRDYO	CTT READY STATUS BIT FROM CTT, LOW ACTIVE
TTRDYOG	GROUND LEAD TWISTED WITH TTRDYO
TTREWCO	TAPE REWIND REQUEST LINE TO THE CTT, ACTIVE LOW
TTREWCOG	GROUND LEAD TWISTED WITH TTREWCO
TTSELO	TRANSPORT SELECT LINE TO THE CTT, ACTIVE LOW
TTSELOG	GROUND LEAD TWISTED WITH TTSELO
TTSFO	SLOW (30 IPS) FORWARD TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TTSFOG	GROUND LEAD TWISTED WITH TTSFO
TTSRO	SLOW (30 IPS) REVERSE TAPE MOTION REQUEST LINE TO THE CTT, ACTIVE LOW
TTSROG	GROUND LEAD TWISTED WITH TTSRO
WRDATA	PHASE ENCODED WRITE DATA INPUT TO THE CTT
WROATAG	GROUND LEAD TWISTED WITH WRDATA
WRENABO	WRITE CIRCUITRY ENABLE REQUEST LINE TO THE CTT (LOGICALLY EQUIVALENT TO WENAAO), ACTIVE LOW
WRENABOG	GROUND LEAD TWISTED WITH WRENABO
WTA00	WRITE TRACK SELECTOR ADDRESS BIT ZERO (LSB), LOW = LOGICAL ONE
WTA00C	GROUND LEAD TWISTED WITH WTA00
WTA10	WRITE TRACK SELECTOR ADDRESS BIT ONE (MSB), LOW = LOGICAL ONE
WTA10G	GROUND LEAD TWISTED WITH WTA10

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

85AB

PRINTED IN U. S. A.

06/15/77

PART OF FS 5
CARTRIDGE TAPE TRANSPORT

SYMBOL NO. 1
CARTRIDGE TAPE TRANSPORT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTT-J6	04-04R	P/O KS-21447,LZ		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		1			TACHTP	
		23			-9V	
		35			ONLINE	
		37			TOR(CC)	
		39			TM	
		41			BOT(CC)	
		43			EOT(CC)	
		45			LPEW(CC)	
		46			CIP	
		48			+9V	
		6			GND	
+24VS	I	50	6/3		+24VS	
+5VB	PWR	24	6/2		+5V	
-48VBS	I	25	6/3		-48V	
-48VRTNB	I	22	6/4		GRD	
CARTWEO	O	49	4/4		CARTWEO	
CARTWEOG	GRD	20			GND	
FRGRD	GRD	21	6/4		GRD	
LPEWO	O	47	4/4		LPEWO	
LPEWOG	GRD	19			GND	
MANENO	I	33	4/4		MANENO	
MANENOG	GRD	13			GND	
RWDINGAO	O	36	4/4		PWDINGAO	
RWDINGOG	GRD	15			GND	
TIMAO	O	40	4/4		TIMAO	
TIMAOG	GRD	17			GND	
TORO	I	38	4/4		TORO	
TOROG	GRD	16			GND	
TTBOTAO	I	42	4/3		BOT	
TTBOTAOG	GRD	7			GND	
TTEOTAO	I	44	4/3		TTEOTAO	
TTEOTAOG	GRD	18			GND	
TTFFO	I	26	4/1		TTFFO	
TTFFOG	GRD	4			GND	
TTFRO	I	28	4/1		TTFRO	
TTFROG	GRD	8			GND	
TTINITO	I	31	4/1		TTINITO	
TTINITOG	GRD	11			GND	
TTMSTPO	I	2	4/1		TTMSTPO	
TTMSTPOG	GRD	3			GND	
TTRDYO	O	34	4/4		TTRDYO	
TTRDYOG	GRD	14			GND	
TTREWCO	I	32	4/1		TTREWCO	
TTREWCOG	GRD	12			GND	
TTSELO	I	30	4/1		TTSELO	
TTSELOG	GRD	10			GND	
TTSFO	I	27	4/1		TTSFO	
TTSFOG	GRD	5			GND	
TTSRO	I	29	4/1		TTSRO	
TTSROG	GRD	9			GND	

SYMBOL NO. 2
CARTRIDGE TAPE TRANSPORT

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
CTT-J5	04-10R	P/O KS-21447,LZ		

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		10			GND	
		11			GND	
		12			GND	
		13			GND	
		17			READTP	
		30			RD(CC)	
		31			RDS(CC)	
		32			DD(CC)	
		33			+PEAKS	
		34			-PEAKS	
		7			GND	
		8			GND	
		9			GND	
OATDETO	O	18	4/4		DATDETO	
DATDETOG	GRD	16			GND	
RDCLKO	O	36	4/2		RDCLKO	
RDCLKOG	GRD	15			GND	
RDDATAO	O	35	4/2		RDDATAO	
RDDATAOG	GRD	14			GND	
RTA00	I	20	4/1		RTA00	
RTA00G	GRD	2			GND	
RTA10	I	22	4/1		RTA10	
RTA10G	GRD	4			GND	
WRDATA	I	24	4/3		WRDATA	
WRDATAG	GRD	6			GND	
WRENABO	OT	23	4/1		WRENABO	
WRENABOG	GRD	5			GND	
WTA00	I	19	4/1		WTA00	
WTA00G	GRD	1			GND	
WTA10	I	21	4/1		WTA10	
WTA10G	GRD	3			GND	

PART OF FS 5
SYMBOL(S) 1 2

TAPE DATA CONTROLLER

DWG SIZE	CZ
ISSUE	5AC
BELL LABORATORIES	SD-1C904-01
	B5CA

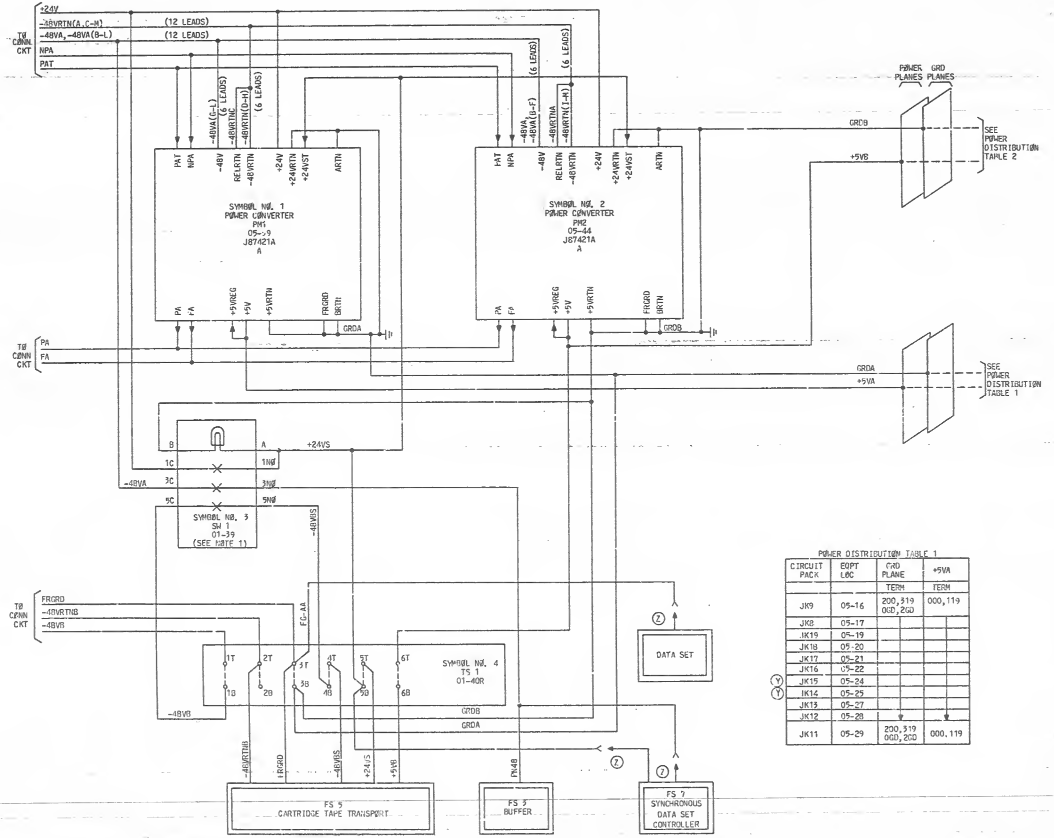
PRINTED IN U. S. A.
07/13/77

PART OF FS 6

POWER
INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. SWITCH S1 IS AN ALTERNATE ACTION SWITCH SUCH THAT IT IS DEPRESSED ONCE TO CLOSE ALL CONTACTS AND DEPRESSED AGAIN TO OPEN ALL CONTACTS.



POWER DISTRIBUTION TABLE 1

	CIRCUIT PACK	EQPT LOC	GRD PLANE	+5VA
			TERM	TERM
	JK9	05-16	200,319 0GD,2GD	000,119
	JK8	05-17		
	JK19	05-19		
	JK18	05-20		
	JK17	05-21		
	JK16	05-22		
Ⓨ	JK15	05-24		
Ⓨ	JK14	05-25		
	JK13	05-27		
	JK12	05-28	↓	↓
	JK11	05-29	200,319 0GD,2GD	000,119

POWER DISTRIBUTION TABLE 2

CIRCUIT PACK	EQPT LOC	GRD PLANE	+5VB
		TERM.	TERM.
JK10	05-31	200,319 0GD,2GD	000,119
JK7	05-32		
JK6	05-33		↓
JK5	05-34		000,119
J87421A	05-39	↓	
J87421A	05-44	200,319 0GD,2GD	

PART OF FS 6
INTERCONNECTION AND FLOW DIAGRAM

TAPE DATA CONTROLLER

DWG SIZE
6S

ISSUE
5AC

BELL LABORATORIES

SD-1C904-01

86AA

PRINTED IN U.S.A.

PART OF FS 6

POWER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+24V	+24 VOLT POWER INPUT BUS
+24VS	+24 VOLT POWER BUS FROM THE TDC POWER SWITCH
+5VA	+5 VOLT POWER BUS A
+5VB	+5 VOLT POWER BUS B
-48VA	-48 VOLT POWER INPUT BUS A
-48VA(B-L)	-48 VOLT POWER BUS A CONNECTIONS TO +5V CONVERTERS
-48VB	-48 VOLT POWER INPUT BUS B
-48VBS	-48 VOLT POWER BUS FROM TDC POWER SWITCH TO CTT (SUPPLIED FROM -48VB)
-48VRTNA	-48 VOLT POWER BUS A GROUND RETURN FROM THE +5V CONVERTERS
-48VRTNB	-48 VOLT POWER BUS B GROUND RETURN FROM CTT
-48VRTN(C-M)	-48 VOLT POWER BUS A GROUND RETURNS FROM +5V CONVERTERS
FA	MAJOR +5V CONVERTER FAILURE ALARM OUTPUT, ACTIVE HIGH
FG-AA	FRAME GROUND TO DATA SET
FRGRD	FRAME GROUND
GRDA	GROUND RETURN FOR +5V POWER BUS A
GRDB	GROUND RETURN FOR +5V POWER BUS B
NPA	+5V CONVERTER POWER ALARM OUTPUT AND POWER ALARM RESET INPUT, ACTIVE LOW
PA	+5V CONVERTER POWER ALARM OUTPUT, ACTIVE HIGH
PAT	+5V CONVERTER POWER ALARM TEST INPUT, LOW ACTIVE
PN48	-48 VOLT POWER FROM TDC POWER SWITCH TO BUF CIRCUIT (SUPPLIED FROM -48VA)

TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
B6AB

PRINTED IN U. S. A.
06/15/77

PART OF FS 6

POWER

SYMBOL NO. 1

POWER CONVERTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PM1	05-39	J87421A	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
+24V	PWR	112	6/2,6/3 TO CONN CKT		+24V	
	PWR	012	6/1		+24V	
+24VS	I	011	6/3		+24VST	
	I	210	6/3		+24VST	
+5VA	OT	001			+5V	
	OT	002			+5V	
	OT	003			+5V	
	OT	004			+5V	
	OT	005			+5V	
	OT	006			+5V	
	OT	007			+5V	
	OT	106			+5V	
	OT	101			+5V	
	OT	102			+5V	
	OT	103			+5V	
	OT	104			+5V	
	OT	105			+5V	
	OT	106			+5V	
	OT	107			+5V	
	I	108			+5VREG	
-48VAG	PWR	119	TO CONN CKT		-48V	
-48VAH	PWR	118	TO CONN CKT		-48V	
-48VAI	PWR	117	TO CONN CKT		-48V	
-48VAJ	PWR	017	TO CONN CKT		-48V	
-48VAK	PWR	018	TO CONN CKT		-48V	
-48VAL	PWR	019	TO CONN CKT		-48V	
-48VRTNC	I	014	TO CONN CKT		RELRTN	
-48VRTND	PWR	015	TO CONN CKT		-48VRTN	
-48VRTNE	PWR	016	TO CONN CKT		-48VRTN	
-48VRTNF	PWR	114	TO CONN CKT		-48VRTN	
-48VRTNG	PWR	115	TO CONN CKT		-48VRTN	
-48VRTNH	PWR	116	TO CONN CKT		-48VRTN	
FA	OT	314	6/2 TO CONN CKT		FA	
GRDA	OT	201			+5VRTN	
	OT	202			+5VRTN	
	OT	203			+5VRTN	
	OT	204			+5VRTN	
	OT	205			+5VRTN	
	OT	206			+5VRTN	
	OT	207			+5VRTN	
	OT	208			BRTN	
	OT	300			+5VRTN	
	OT	301			+5VRTN	
	OT	302			+5VRTN	
	OT	303			+5VRTN	
	OT	304			+5VRTN	
	OT	305			+5VRTN	
	OT	306			+5VRTN	
	OT	307			+5VRTN	
	I	013			ARTN	
	I	113			ARTN	
	GRD	111			+24VRTN	
	GRD	319		203	FRGRD	
GRDB	GRD	0GD		203	FRGRD	
	GRD	2GD		203	FRGRD	
	GRD	200		203	GRD	
	GRD	319		203	FRGRD	

SYMBOL NO. 1 (CONT)

POWER CONVERTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PM1	05-39	J87421A	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
NPA	I	315	6/2 TO CONN CKT		NPA	
PA	OT	313	6/2 TO CONN CKT		PA	
PAT	I	312	6/2 TO CONN CKT		PAT	

SYMBOL NO. 2

POWER CONVERTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PM2	05-44	J87421A	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
+24V	PWR	012	6/1		+24V	
	PWR	112	6/1		+24V	
+24VS	I	011	6/3		+24VST	
	I	210	6/3		+24VST	
+5VB	OT	001	5/1,6/4		+5V	
	OT	002	6/2		+5V	
	OT	003	6/2		+5V	
	OT	004	6/2		+5V	
	OT	005	6/2		+5V	
	OT	006	6/2		+5V	
	OT	007	6/2		+5V	
	OT	100	6/2		+5V	
	OT	101	6/2		+5V	
	OT	102	6/2		+5V	
	OT	103	6/2		+5V	
	OT	104	6/2		+5V	
	OT	105	6/2		+5V	
	OT	106	6/2		+5V	
	OT	107	6/2		+5V	
	I	108	6/2		+5VREG	
-48VA	PWR	019	6/3 TO CONN CKT		-48V	
-48VAB	PWR	018	TO CONN CKT		-48V	
-48VAC	PWR	017	TO CONN CKT		-48V	
-48VAD	PWR	117	TO CONN CKT		-48V	
-48VAE	PWR	118	TO CONN CKT		-48V	
-48VAF	PWR	119	TO CONN CKT		-48V	
-48VRTNA	I	014	TO CONN CKT		RELRTN	
-48VRTNI	PWR	015	TO CONN CKT		-48VRTN	
-48VRTNJ	PWR	016	TO CONN CKT		-48VRTN	
-48VRTNK	PWR	116	TO CONN CKT		-48VRTN	
-48VRTNL	PWR	115	TO CONN CKT		-48VRTN	
-48VRTNM	PWR	114	TO CONN CKT		-48VRTN	
FA	OT	314	6/1		FA	
GRDB	OT	201	6/2		+5VRTN	
	OT	202	6/2		+5VRTN	
	OT	203	6/2		+5VRTN	
	OT	204	6/2		+5VRTN	
	OT	205	6/2		+5VRTN	
	OT	206	6/2		+5VRTN	

SYMBOL NO. 2 (CONT)

POWER CONVERTER

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
PM2	05-44	J87421A	A	

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
GRDB	OT	207	6/2		+5VRTN	
	OT	208			BRTN	
	I		6/3			
	OT	300	6/2		+5VRTN	
	OT	301	6/2		+5VRTN	
	OT	302	6/2		+5VRTN	
	OT	303	6/2		+5VRTN	
	OT	304	6/2		+5VRTN	
	OT	305	6/2		+5VRTN	
	OT	306	6/2		+5VRTN	
	OT	307	6/2		+5VRTN	
	I	013	6/2		ARTN	
	I	113	6/2		ARTN	
	GRD	0GD		203	FRGRD	
	GRD	111			+24VRTN	
	GRD	2GD		203	FRGRD	
	GRD	200		203	FRGRD	
	GRD	319	TO CONN CKT	203	FRGRD	
NPA	I	315	6/1		NPA	
PA	OT	313	6/1		PA	
PAT	I	312	6/1		PAT	

SYMBOL NO. 3

POWER SWITCH

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SW1	01-39	(NOTE 206)		

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
+24V	PWR	1C	6/1			
+24VS	OT	A	(Z)7/2			
	I		5/1,6/1 6/2,6/4			
	OT	1NO	6/3			
-48VA	PWR	3C	6/2			
-48VB	I	5C	6/4			
-48VBS	O	5NO	5/1,6/4			
GRDB	I	B	6/2			
PN48	O	3NO	3/3,(Z)7/2			

SYMBOL NO. 4

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
TS1	01-40R	KS-20856,L6		

LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
			FS INFO		CP INFO	
+24VS	I	5B	6/3			
	I	5T	6/3			
+5VB	PWR	6B	6/2			
	PWR	6T	6/2			
-48VB	I	1B	6/3			
	I	1T	6/3 TO CONN CKT			
-48VBS	I	4B	6/3			
	I	4T	6/3			
-48VRTNB	I	2B	5/1			
	I	2T	5/1 TO CONN CKT			
FG-AA	GRD	3T	TO CONN CKT			
FRGRD	GRD	3T	5/1 TO CONN CKT			
GRDA	GRD	3B				
GRDB	GRD	3B				

PART OF FS 6
SYMBOL(S) 1 2 3 4

TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
B6CA
PRINTED IN U. S. A.
07/13/77

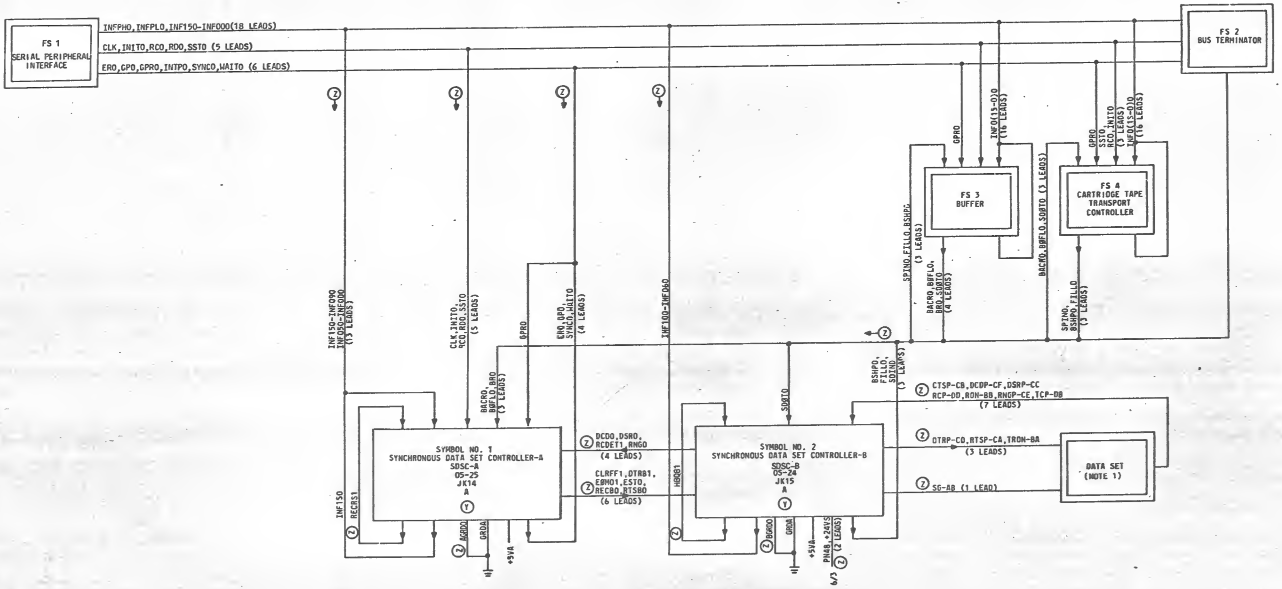
PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER INTERCONNECTION AND FLOW DIAGRAM

NOTES:

1. REFER TO APPROPRIATE SD FOR INFORMATION ON USER SUPPLIED DATA SET. RECOMMENDED NEW FAMILY DATA SETS WITH WHICH THE SDSC IS COMPATIBLE ARE:

201C 2400 BPS, SWITCHED NETWORK OR PRIVATE LINE
208A 4800 BPS, 4 WIRE PRIVATE LINE
208B 4800 BPS, SWITCHED NETWORK
209A 9600 BPS, 4 WIRE PRIVATE LINE



PART OF FS 7
INTERCONNECTION AND FLOW DIAGRAM

DATA TAPE CONTROLLER	DWG SIZE 6S	ISSUE 5AC
BELL LABORATORIES	SD-1C904-01	B7AA

PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
+24VS	+24 VOLT POWER BUS FROM THE TDC POWER SWITCH
+5VA	+5 VOLT POWER BUS A
AGRD0	GROUND STRAP
BACR0	SERIAL BUFFER BUS CARRY PULSE INDICATING THAT THE ON-LINE (ACTIVE) DATA BUFFER HAS BEEN EITHER FILLED OR EMPTIED, ACTIVE LOW
BGRD0	GROUND STRAP
BOFL0	SERIAL BUFFER BUS OVERFLOW INDICATION, ACTIVE LOW
BR0	OFF-LINE BUFFER READY FOR SERVICING FLAG, ACTIVE LOW
BSHP0	SERIAL BUFFER BUS DATA SHIFT PULSE, ACTIVE LOW
CLK	COMMON PARALLEL BUS SQUARE WAVE CLOCK PULSE TRAIN WITH 600 NS PERIOD
CLRFF1	CLEAR THE FILL FLIP-FLOP, ACTIVE HIGH
CTSP-CB	CLEAR TO SEND EIA LEVEL FROM DATA SET
DCDP-CF	RECEIVED CARRIER DETECT FROM DATA SET
DCD0	RECEIVED CARRIER DETECT, ACTIVE LOW
DSRP-CC	DATA SET READY EIA LEVEL FROM DATA SET
DSR0	DATA SET READY, ACTIVE LOW
DTRB1	DATA TERMINAL READY, ACTIVE HIGH
DTRP-CD	DATA TERMINAL READY EIA LEVEL TO DATA SET
EOMP1	END OF MESSAGE PULSE, ACTIVE HIGH
ER0	REQUEST TO THE SPI TO TRANSMIT AN ERROR START CODE IN THE CURRENT STATUS REPLY TO THE CC, LOW ACTIVE
EST0	ENABLE SDSC STATUS REPLY, ACTIVE LOW
FILL0	SERIAL BUFFER BUS FILL OPERATION REQUEST, ACTIVE LOW
GPR0	REPLY FROM BT TO ACKNOWLEDGE THE RECEIPT OF A GPO REQUEST, ACTIVE LOW
GP0	REQUEST TO BT TO GENERATE PARITY OVER THE STATUS REPLY CURRENTLY RESIDING ON THE COMMON PARALLEL BUS
HBQ87	STRAP BETWEEN INPUT REGISTERS
INF(00-15)0	COMMON PARALLEL BUS BITS (00-15) LOW = LOGICAL ONE
INIT0	TDC INITIALIZE COMMAND, LOW ACTIVE
PN48	-48 VOLT POWER FROM TDC POWER SWITCH TO BUF CIRCUIT (SUPPLIED FROM -48VA)
RCDET1	RECEIVE CLOCK DETECT, ACTIVE HIGH
RCP-DD	RECEIVE CLOCK EIA PULSE TRAIN FROM DATA SET
RC0	ADDRESS DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS AND INTERPRET THEM AS A COMMAND, LOW, ACTIVE
RDN-BB	RECEIVE DATA EIA PULSE TRAIN FROM DATA SET
RD0	ADDRESSED DEVICE TO RECEIVE THE DATA ON THE COMMON PARALLEL BUS, ACTIVE LOW

SYMBOL/LEAD DESIGNATION

MNEMONIC	DEFINITION
RECB0	RECEIVE ENABLE, ACTIVE LOW
RECRS1	RECEIVE STATE RESET PULSE, ACTIVE HIGH (STRAP)
RNGP-CE	RINGING EIA LEVEL FROM DATA SET
RNG0	TEL SET RINGING, ACTIVE LOW
RTSB0	REQUEST TO SEND, ACTIVE LOW
RTSP-CA	REQUEST TO SEND EIA LEVEL TO DATA SET
SDIN0	SERIAL BUFFER BUS DATA INPUT TO THE BUFFER UNIT, LOW = LOGICAL ONE
SDOT0	SERIAL BUFFER BUS DATA OUTPUT FROM THE BUFFER UNIT LOW = LOGICAL ONE
SG-AB	SIGNAL GROUND TO DATA SET
SST0	ADDRESSED DEVICE REQUESTED TO GATE A STATUS REPLY ON THE COMMON PARALLEL BUS, ACTIVE LOW
SYNC0	A SYNCHRONIZING SIGNAL TO THE SPI WHICH INDICATES THAT A DEVICE HAS SENSED A COMMAND ON THE PARALLEL BUS, ACTIVE LOW
TCP-DB	TRANSMIT CLOCK EIA PULSE TRAIN FROM DATA SET
TRDN-BA	TRANSMIT DATA EIA PULSE TRAIN TO DATA SET
WAIT0	A REQUEST TO THE SPI TO WAIT UNTIL THE DEVICE HAS HAD TIME TO ACT UPON A COMMAND BEFORE REMOVING THAT COMMAND FROM THE COMMON PARALLEL BUS, ACTIVE LOW

TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
87AB
PRINTED IN U. S. A.
06/15/77

PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER

SYMBOL NO. 1

SYNCHRONOUS DATA SET CONTROLLER-A

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SDSC-A	05-25	JK14	A	(Y)

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
+5VA	PWR	000		203	+5	
	PWR	119		203	+5	
AGRD0	I	306	(2)7/1		AGRD0	3A5
	GRD	200			GRD	
BACR0	I	018	3/4		BACR0	3A1
BOFL0	I	313	3/2		BOFL0	2A4
BR0	I	015	3/2		BR0	2A6
CLK	I	103	1/3		CLK	2A8
CLRFF1	O	203	(2)7/2		CLRFF1	3H1
OCD0	I	204	(2)7/2		DCD0	3A8
DSR0	I	108	(2)7/2		DSR0	3A9
DTRB1	O	003	(2)7/2		DTRB1	3H9
EOMP1	O	100	(2)7/2		EOMP1	3H6
ER0	OT	117	2/1		ER0	2H1
EST0	O	213	(2)7/2		EST0	2H5
GPR0	I	101	2/1		GPR0	2A6
GP0	OT	202	3/1		GP0	2H7
GRDA	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203	GRD	
	GRD	319		203	GRD	
INF000	I	215	1/1		INF000	2A2
INF010	I	314	1/1		INF010	2A2
INF020	I	211	1/1		INF020	2A1
INF030	I	310	1/1		INF030	2A1
INF040	I	116	1/1		INF040	2A0
INF050	I	214	1/1		INF050	2A0
INF090	I	305	1/1		INF090	3A5
INF100	I	010	1/1		INF100	3A4
INF110	I	109	1/1		INF110	3A2
INF120	I	207	1/1		INF120	3A1
INF130	I	307	1/1		INF130	3A0
INF140	I	312	1/1		INF140	2A5
INF150	OT	212	1/1		INF150	3H8
INIT0	I	318	1/3		INIT0	2A2
RCDET1	I	302	(2)7/2		RCDET1	3A6
RC0	I	216	1/3		RC0	2A3
RD0	I	007	1/3		RD0	2A3
RECB0	O	019	(2)7/2		RECB0	3H5
RECRS1	I	201	(2)7/1		RECRS1	3A4
	O	301			RECRS1	3A4
RNG0	I	008	(2)7/2		RNG0	3A8
RTSB0	O	001	(2)7/2		RTSB0	3HA
SST0	I	217	1/3		SST0	2A7
SYNC0	OT	303	2/1		SYNC0	2H1
WAIT0	OT	104	2/1		WAIT0	2H6

SYMBOL NO. 2

SYNCHRONOUS DATA SET CONTROLLER-B

DESIG	EQPT LOC	CODE	ELEM IDENT	OPT
SDSC-B	05-24	JK15	A	(Y)

FS INFO					CP INFO	
LEAD DESIG	FUNC	TERM.	DESTINATION	NOTE	TERM. MOD	LOC
		004			-12V	3B4
		202			+12V	3B3
+24VS	PWR	003	6/3		+24VS	3B3
+5VA	PWR	000		203	+5	
	PWR	119		203	+5	
BGRD0	I	306	(2)7/2		BGRD0	2A6
	GRD	200			GRD	
BSHP0	OT	019	4/3		BSHP0	2H7
CLRFF1	I	114	(2)7/1		CLRFF1	2A0
CTSP-CB	I	218	TO CONN CKT		CTSP-CB	2A8
OCDP-CF	I	313	TO CONN CKT		DCDP-CF	3B1
OCD0	O	113	(2)7/1		DCD0	3G0
DSRP-CC	I	317	TO CONN CKT		DSRP-CC	3B2
DSR0	O	217	(2)7/1		DSR0	3G2
DTRB1	I	008	(2)7/1		DTRB1	3B5
DTRP-CD	O	310	TO CONN CKT		DTRP-CD	3G5
EOMP1	I	115	(2)7/1		EOMP1	2A0
EST0	I	209	(2)7/1		EST0	2A6
FILL0	OT	016	4/3		FILL0	2H0
GRDA	GRD	0GD		203		
	GRD	2GD		203		
	GRD	200		203	GRD	
	GRD	319		203	GRD	
HBQ81	I	309	(2)7/2		HBQ81	2A4
	O	012			HBQ81	2H6
INF060	OT	205	1/1		INF060	2H3
INF070	OT	304	1/1		INF070	2H3
INF080	OT	206	1/1		INF080	2H4
INF090	OT	305	1/1		INF090	2H2
INF100	OT	010	1/1		INF100	2H5
PN48	I	002	6/3		PN48	3B4
RCDET1	O	015	(2)7/1		RCDET1	2H1
RCP-DD	I	213	TO CONN CKT		RCP-DD	2A1
RDN-BB	I	214	TO CONN CKT		RDN-BB	2A2
RECB0	I	111	(2)7/1		RECB0	2A2
RNGP-CE	I	314	TO CONN CKT		RNGP-CE	3B1
RNG0	O	316	(2)7/1		RNG0	3G1
RTSB0	I	108	(2)7/1		RTSB0	2A7
RTSP-CA	O	106	TO CONN CKT		RTSP-CA	2H9
SDIN0	OT	117	3/2		SDIN0	2H5
SDOT0	I	014	3/4		SDOT0	2A8
SG-AB	GRD	210	TO CONN CKT		SG-AB	3G6
TCP-DB	I	318	TO CONN CKT		TCP-DB	2A6
TRDN-BA	O	105	TO CONN CKT		TRDN-BA	2H8

PART OF FS 7
SYMBOL(S) 1 2

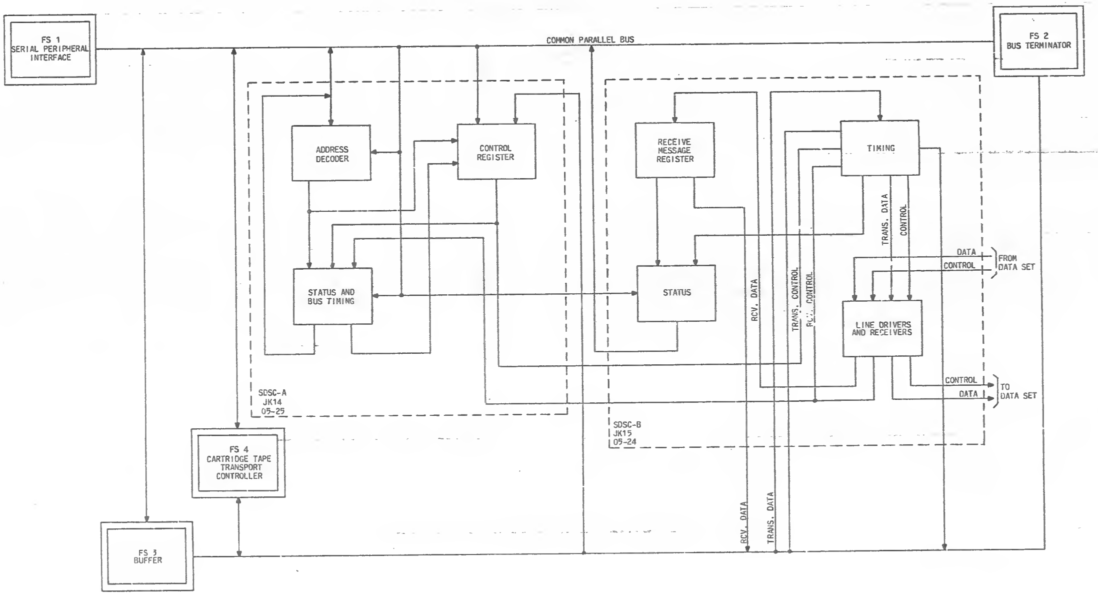
TAPE DATA CONTROLLER
DWG SIZE C2
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
B7CA
PRINTED IN U. S. A.
07/13/77

PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER

COMPOSITE DIAGRAM I

FUNCTIONAL DIAGRAM OF SDSC



PART OF FS 7
COMPOSITE DIAGRAM 1

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 5AC
BELL LABORATORIES	SD-1C904-01	B7GA

PART OF FS 7
SYNCHRONOUS DATA SET CONTROLLER

COMPOSITE DIAGRAM 2
DESCRIPTION OF OPERATION

1. GENERAL INFORMATION

1.1 THE SDSC CIRCUIT PACKS ARE A USER SPECIFIED OPTION TO THE TDC CIRCUIT AND MAY BE PURCHASED SEPARATELY. TDC'S BUILT AFTER MID 1977 WILL HAVE BACKPLANE WIRING FACTORY INSTALLED. WIRING LISTS ARE AVAILABLE FOR USERS WISHING TO RETROFIT EXISTING TDCS. THE SDSC IS REQUIRED FOR 2B ESS OFFICES USING THE EF2 GENERIC.

1.2 THE SDSC SENDS AND RECEIVES EIA STANDARD SIGNALS FOR USE BY A USER SUPPLIED DATA SET WHICH MAY BE LOCATED UP TO 50 WIRE FEET AWAY FROM THE TDC. THE TDC BACKPLANE CONTAINS A KS-19088,L14 CONNECTOR TO MATE WITH ALL EIA BINARY SYNCHRONOUS HALF DUPLEX DATA SETS WITH A USER SUPPLIED CABLE.

1.3 THE SDSC HAS THE CAPABILITY TO OPERATE AT 2K,2.4K,4.8K AND 9.6K BITS PER SECOND. NO ALTERATION OF THE SDSC IS REQUIRED TO OPERATE AT THE VARIOUS DATA RATES. IT IS NECCESSARY THAT SPEED AND FUNCTION COMPATIBLE DATA SETS BE USED AT OPPOSITE ENDS OF THE DATA LINK.

1.4 PRIOR TO ATTACHING A DATA SET TO THE SDSC THE FOLLOWING OPTIONS INTERNAL TO THE DATA SET SHOULD BE CHECKED PER THE APPROPRIATE BSP. ALL OTHER OPTIONS AS SUPPLIED BY THE FACTORY.

1.4.1. GROUNDING - FOR ESS USE FRAME GROUND MUST BE SEPARATED FROM SIGNAL GROUND.
1.4.2. AUTOMATIC ANSWER - PER PROGRAM REQUIREMENTS
1.4.3. TRANSMIT LINE SIGNAL LEVEL - PER OFFICE REQUIREMENTS

1.5 THE SDSC WILL ONLY OPERATE IN HALF-DUPLEX MODE. E.G. IT MAY NOT BE USED TO SIMULTANEOUSLY TRANSMIT AND RECEIVE.

1.6 THE SDSC IS TRANSPARENT TO THE PROTOCOL USED. IT IS ALSO TRANSPARENT TO THE DATA TRANSMITTED WITH THE EXCEPTION OF THE FIRST CHARACTERS WHICH MUST BE EIA STANDARD SYN CHARACTERS. THESE ARE USED FOR MESSAGE DETECTION AND DISCARDED. ALL OTHER DATA MANIPULATIONS MUST BE DONE BY THE PROGRAM.

2. CALLING SEQUENCE (NUMBERS IN CIRCLES REFER TO POINTS IN FIG. 1)

2.1 ① LINE INACTIVE, TRANSMIT CLOCK IS ALWAYS PRESENT FROM THE DATA SETS TO THE CUSTOMER EQUIPMENT (SDSC) AT BOTH ENDS OF THE LINE.

2.2 THE CALLING END HAS DIALED AND THE CALLED PHONE IS RINGING ② THE LINE LIGHT ON THE CALLED PHONE IS FLASHING.

2.3 THE LINE KEY IS DEPRESSED ③ (PLACING THE PHONE IN THE VOICE MODE), THE HANDSET IS PICKED UP, AND VOICE CONTACT IS ESTABLISHED.

2.4 THE FIRST PROGRAM ACTION TAKEN IS TO SET DATA TERMINAL READY ④ THE "TR" LAMP ON A 201-C DATA SET WILL BE LIT WHEN DTR IS ACTIVE.

2.5 THE DATA (RELEASE) KEY ON THE TEL. SET IS THEN DEPRESSED ⑤ THE LINE LIGHT SHOULD THEN ILLUMINATE AND THE HANDSET MAY BE HUNG UP WITHOUT DROPPING THE LINE.

2.6 APPROXIMATELY 53ms LATER THE DATA SET WILL ACTIVATE ITS READY BIT ⑥ INDICATING DATA MODE AND ILLUMINATE THE "MR" LAMP (201-C).

2.7 THE ON STATE OF THE "MR" LAMP SHOULD NOT BE INTERPRETED TO MEAN THAT A DATA COMMUNICATIONS PATH EXISTS. THE CALLING STATION MUST ALSO BE IN THE DATA MODE.

2.8 EITHER END MAY INITIATE A DATA TRANSFER (DEPENDING UPON THE PROTOCOL) BUT FOR THE SAKE OF THIS EXAMPLE WE WILL ASSUME THE CALLING END DOES SO.

2.9 THE CALLED (RECEIVING) END MUST SET ITS' RECEIVE BIT ⑦ ENABLING THE RECEIVE MESSAGE REGISTER AND THE CALLING (TRANSMITTING) END THEN SETS ITS TRANSMIT BIT WHICH ASSERTS REQUEST TO SEND TO THE DATA SET ⑧.

2.10 150ms LATER THE CALLING DATA SET REPLIES TO ITS' SDSC WITH A CLEAR TO SEND ⑨.

2.11 APPROXIMATELY 5ms LATER ⑩ THE CARRIER SENT BY THE CALLING END IS RECEIVED AND SYNCHRONIZED BY THE CALLED DATA SET WHICH BEGINS TO SEND CLOCK INFORMATION AND CARRIER DETECT TO THE CALLED SDSC.

2.12 ANY TIME AFTER CTS GOES ACTIVE THE CALLING SDSC IS FREE TO SEND DATA TO ITS' DATA SET ⑪ USING THE TRANSMIT CLOCK TO SHIFT DATA FROM THE TDC BUFFER CIRCUIT.

2.13 AFTER DETECTING TWO SYN CHARACTERS (026 OR 226) ⑫ THE CALLED SDSC INDICATES SYNCHRONIZATION (INF 060).

2. CALLING SEQUENCE (CONT)

2.14 AS THE FIRST NON-SYN CHARACTER IS DETECTED THE SDSC WILL ASSERT "NEW MESSAGE" ⑬ (INF070)

2.15 AS THE CALLING END SENDS THE END OF ITS MESSAGE ⑭ IT MAY DISABLE REQUEST TO SEND EITHER MANUALLY OR AUTOMATICALLY VIA THE ABE BIT. THIS IS IMMEDIATELY REFLECTED BY THE DATA SET REMOVING CLEAR TO SEND.

2.16 THE TRANSMITTING DATA CONTINUES TO RUN FOR SEVERAL CLOCK CYCLES ⑮ CLEARING ITS' INTERNAL REGISTERS OF ANY REMAINING BITS.

2.17 THE RECEIVING DATA SET SIMILARLY CONTINUES TO RUN FOR SEVERAL CYCLES ⑯ FOR THE SAME REASON AND THEN DISABLES CARRIER DETECT TO THE CALLED SDSC.

2.18 THE SDSC SEES DCD GO AWAY AND REMOVES THE RECEIVE CLOCK (IF STILL PRESENT) CAUSING NEW MESSAGE AND SYNC TO GO INACTIVE. THIS TRIGGERS AN END OF MESSAGE PULSE AND FORCES A FILL OF THE TDC BUFFER CIRCUIT IF THE BUFFER READY FLAG IS NOT SET.

2.19 IF THE ACTION ON BUFFER END (ABE) BIT WAS SET IN THE TRANSMITTING SDSC; THE ACTION OF EMPTYING THE LAST BIT FROM THE BUFFER CIRCUIT WILL CLEAR THE TRANSMIT STATE (RTS) AND SET THE RECEIVE STATE. ⑰ THIS OPENS THE LINE FOR TRANSMISSION IN THE REVERSE DIRECTION WHICH OCCURS IN THE SAME MANNER AS DESCRIBED IN 2.9 - 2.18.

2.20 COMMUNICATIONS TYPICALLY CONTINUE LIKE THIS WITH REPETITIVE LINE REVERSALS UNTIL ALL DATA IS TRANSMITTED ⑲.

2.21 DATA TRANSFER MAY BE INTERRUPTED AT ANY TIME TO RE-ESTABLISH VOICE CONTACT (SEE FIG. 2) OR TERMINATE THE CALL. TRANSFER TO VOICE MODE OR CALL TERMINATION MUST OCCUR AT BOTH ENDS OF THE LINE.

2.22 THE CALL IS TERMINATED BY EITHER ⑳ TRANSFERING TO VOICE MODE AND HANGING UP OR, IF THE DATA SET IS OPTIONED FOR DTR CONTROL, BY REMOVING DATA TERMINAL READY ㉑.

2.23 THE LINE IS ACTUALLY TERMINATED 15ms LATER ㉒ WHEN DATA SET READY GOES INACTIVE.

PART OF FS 7
COMPOSITE DIAGRAM 2

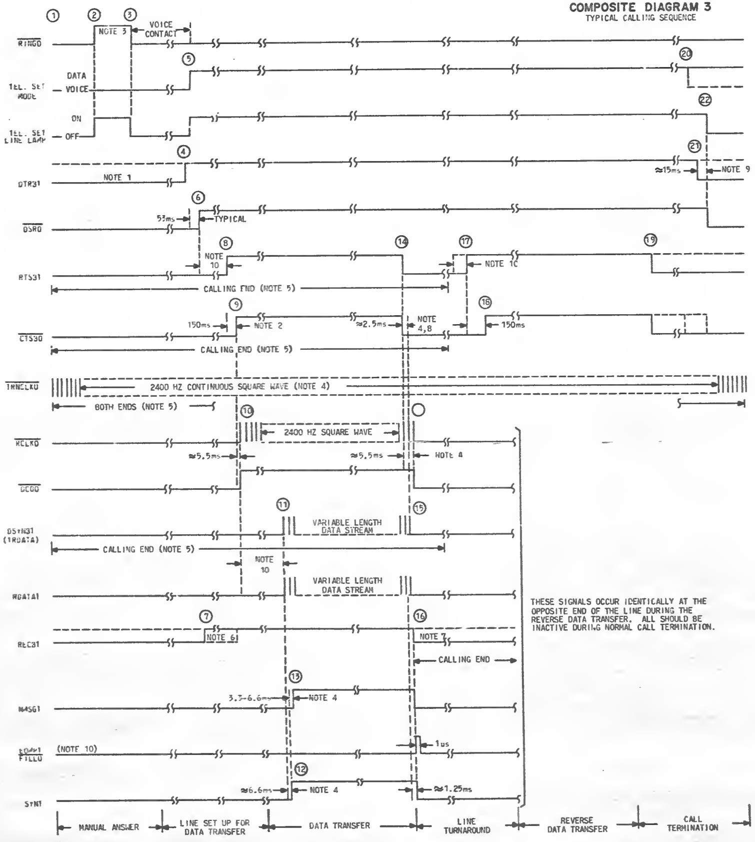
TAPE DATA CONTROLLER
DWG SIZE 6S
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
87GB

PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER

COMPOSITE DIAGRAM 3

TYPICAL CALLING SEQUENCE



THESE SIGNALS OCCUR IDENTICALLY AT THE OPPOSITE END OF THE LINE DURING THE REVERSE DATA TRANSFER. ALL SHOULD BE INACTIVE DURING NORMAL CALL TERMINATION.

FIGURE I

NOTES:

1. THE POINT AT WHICH DTR IS SET IS NOT CRITICAL AS LONG AS IT IS ACTIVE PRIOR TO PUTTING THE TEL SET INTO DATA MODE.
2. OPTION SELECTABLE.
3. RINGO IS ONLY ACTIVE AT THE TIME THE CALLED TEL SET IS ACTUALLY RINGING (THE SAME TIME AS THE TEL SET LINE LAMP IS LIT).
4. TIMING FOR 201C DATA SET ON 2 WIRE SWITCHED NETWORK ONLY.
5. UNLESS OTHERWISE STATED, SIGNALS SHOWN ARE THE CALLED END OF THE LINE (THE END WHICH RECEIVES THE FIRST MESSAGE).
6. RECB1 MUST BE SET PRIOR TO RDATA1 GOING ACTIVE AND SHOULD BE SET PRIOR TO DCDO GOING ACTIVE.
7. RECB1 IS ASSERTED BY THE CALLING END AUTOMATICALLY IF ABE WAS SENT.
8. ALTHOUGH CTS GOES INACTIVE SIMULTANEOUSLY WITH RTS THERE IS AN EFFECTIVE INTERVAL OF 1-2ms WHEN RTS MAY BE REASSERTED WITHOUT INVOKING THE NORMAL 150ms DELAY.
9. LINE DISCONNECT IS ACHIEVED IN DATA MODE BY REMOVING DTR, OR IN VOICE MODE BY HANGING UP THE HANDSET.
10. DELAY INDICATED AT THESE POINTS IS VARIABLE AND A FUNCTION OF PROGRAM TIMING.

PART OF FS 7
COMPOSITE DIAGRAM 3

TAPE DATA CONTROLLER	DWG SIZE 6S	ISSUE 5AC
BELL LABORATORIES	SD-1C904-01	B7GC

PART OF FS 7

SYNCHRONOUS DATA SET CONTROLLER

COMPOSITE DIAGRAM 4

CALL ORIGINATION AND TERMINATION FLOW CHART

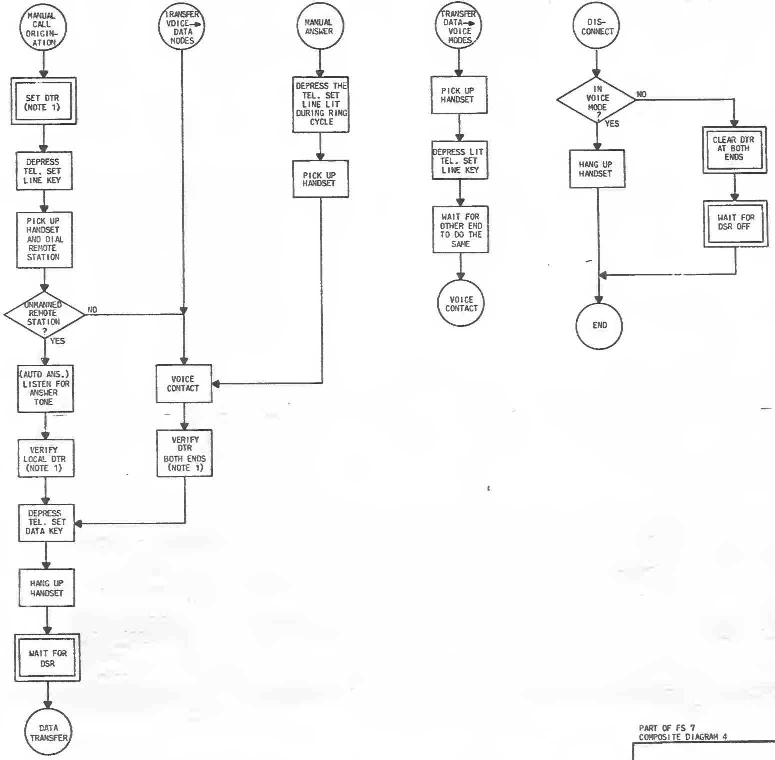
3. CALL ORIGINATION AND TERMINATION

3.1 A CALL MAY BE ORIGINATED EITHER MANUALLY AS SHOWN IN FIGURE 1, OR AUTOMATICALLY WITH AN AUTOMATIC CALLING UNIT (ACU). THE ACU MUST BE INTERFACED SEPARATELY FROM THE DATA SET.

3.2 SIMILARLY A CALL MAY BE ANSWERED MANUALLY AS PREVIOUSLY DESCRIBED, OR MAY BE AUTOMATICALLY ANSWERED BY THE DATA SET. THIS WILL OCCUR IF THE DATA SET IS OPTIONED FOR LINE CONTROL BY DTR (SEE APPROPRIATE DATA SET BSP) AND THE TEL. SET IS IN DATA MODE WITH DTR SET WHEN RNGO IS ACTIVE.

NOTES:

1. THE ACTUAL POINT AT WHICH DTR IS SET IS NOT CRITICAL AS LONG AS IT IS SET PRIOR TO TRANSFERRING INTO DATA MODE.
2. DOUBLED BORDERED BOXES INDICATE SYSTEM SOFTWARE ACTION.


MANUAL CALL ORIGINATION
SET DTR (NOTE 1)
DEPRESS TEL. SET LINE KEY
PICK UP HANDSET AND DIAL REMOTE STATION
UNMANNED REMOTE STATION ?
NO
YES
(AUTO ANS.) LISTEN FOR ANSWER TONE
VERIFY LOCAL DTR (NOTE 1)
DEPRESS TEL. SET DATA KEY
HANG UP HANDSET
WAIT FOR DSR
DATA TRANSFER
TRANSFER VOICE→DATA MODES
VOICE CONTACT
VERIFY DTR BOTH ENDS (NOTE 1)
MANUAL ANSWER
DEPRESS THE TEL. SET LINE LIT DURING RING CYCLE
PICK UP HANDSET
TRANSFER DATA→VOICE MODES
PICK UP HANDSET
DEPRESS LIT TEL. SET LINE KEY
WAIT FOR OTHER END TO DO THE SAME
VOICE CONTACT
DIS-CONNECT
IN VOICE MODE ?
NO
YES
HANG UP HANDSET
CLEAR DTR AT BOTH ENDS
WAIT FOR DSR OFF
END

PART OF FS 7
COMPOSITE DIAGRAM 4

TAPE DATA CONTROLLER

DWG SIZE 6S

ISSUE 5AC

BELL LABORATORIES

SD-1C904-01

B7GD

APP FIG. 1

CIRCUIT PACK

EQPT LOC	05-16	05-17	05-19	05-20	05-21	05-22	05-27	05-28	05-29	05-31	05-32	05-33	05-34	EQPT LOC
DESIG	BT-B	BT-A	CTTC-D	CTTC-C	CTTC-B	CTTC-A	BUF-D	BUF-C	BUF-B	BUF-A	SPI-C	SPI-B	SPI-A	DESIG
CODE	JK9	JK8	JK19	JK18	JK17	JK16	JK13	JK12	JK11	JK10	JK7	JK6	JK5	CODE
OPTION														OPTION
ELEM IDENT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	CKT	ELEM IDENT
CKT	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	DESIG FS/SYM	CKT
A	2/2	2/1	4/4	4/3	4/2	4/1	3/4	3/3	3/2	3/1	1/3	1/2	1/1	A

CT TRANSPORT

OPTION	DESIG	FS/SYM	CODE
	CTT-J5	5/2	P/O KS-21447,L2
	CTT-J6	5/1	P/O KS-21447,L2

POWER MODULE

OPTION	DESIG	FS/SYM	CODE
	PM1	6/1	J87421A
	PM2	6/2	J87421A

SWITCH

OPTION	DESIG	FS/SYM	CODE
	SW1	6/3	(NOTE 206)

APP FIG. 2

CIRCUIT PACK

EQPT LOC	05-24	05-25	EQPT LOC
DESIG	SDSC-B	SDSC-A	DESIG
CODE	JK15	JK14	CODE
OPTION	Y	Y	OPTION
ELEM IDENT	CKT	CKT	ELEM IDENT
CKT	DESIG FS/SYM	DESIG FS/SYM	CKT
A	7/2	7/1	A

ISSUE
5AC

TAPE DATA CONTROLLER

BELL TELEPHONE LABORATORIES
INCORPORATED

DWG SIZE
C2

SD-1C904-01-C1

CIRCUIT NOTES:

101.

DESIG	FUSE AMP	POTENTIAL	ONE PER
-48VA	1-1/3	-48	APP FIG. 1
-48VB	2	-48	
+24V	3/4	+24	

BATTERY SYMBOL	VOLTAGE RANGE
+24	20.75-26.25
-48	42.75-52.5

102.

FEATURE OR OPTION		PROVIDE		
		APP FIG.	APP OR WRG	QUANTITY
TAPE DATA CONTROLLER		1		1 PER CKT
SYNCHRONOUS DATA SET CONTROLLER	APPARATUS	2	Y	1 PER CKT
	WIRING ALWAYS REQD		Z	

103.

RECORD OF FIGURES, WIRING AND APPARATUS CHANGES						
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT		
				STD	A&M	MD
5AC	Y OR Z	NONE		Y AND Z		

EQUIPMENT NOTES:

201. UNLESS OTHERWISE SPECIFIED, ALL WIRING SHALL BE 30 GAUGE, AUTOMATICALLY INSTALLED, D-4 TYPE WIRING.

202. WIRING SHALL BE KS-21337 30 GAUGE TIGHT TWISTED PAIR.

203. PART OF ED-4C017-30 MULTILAYER BACKPLANE.

206. MASTER SPECIALTIES CO. SWITCH PART NO. 600-A8-C3-D1-F14-J1W-L3.

207. THE DATA SET MAY BE LOCATED IN ANY SPACE AVAILABLE AS LONG AS THE CONNECTING CIRCUIT CABLE DOES NOT EXCEED 50 FEET IN LENGTH.

INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.

302. IN SDSC APPLICATIONS OF THE TDC REFER TO APPROPRIATE SD FOR INFORMATION ON USER SUPPLIED DATA SET. SEE NOTE 1 ON FS 7 FOR SDSC COMPATIBLE RECOMMENDED DATA SETS.

ISSUE
5AC

TAPE DATA CONTROLLER
②
SD-1C904-01-D1

BELL TELEPHONE LABORATORIES
INCORPORATED
6S

NOTES:

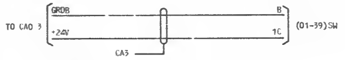
1. UNLESS OTHERWISE SPECIFIED WIRING SHALL BE 26 GA, BY, TIGHT TWISTED PAIR.
2. WIRING SHALL BE 16 GA, KS-13385 STRANDED WIRE.
3. WIRING SHALL BE 18 GA, KS-13385 STRANDED WIRE.
4. WIRING SHALL BE 20 GA, BW TYPE WIRE.
5. WIRING SHALL BE 22 GA, BU TYPE WIRE.
6. WIRING SHALL BE KS-21336, 28 GA WIRE.
7. WIRING SHALL BE KS-21336, 30 GA WIRE.
8. WIRE METHOD OF CA3 IS DEFINED AS PART OF CABLE ASSEMBLY ED4C084-10.
9. THE FOLLOWING CODES OF CONNECTORS ARE USED:

J1-J6	KS-20863,L1; MATING CABLE CONNECTOR KS-20864,L9.
J7,J8	943AJ
J9	KS-16785,L11
J10	KS-16785,L15
J11-J13	942C
J14,J15	943AJ
J16	KS-19088,L14:MATING CABLE CONNECTOR KS-19087, L7

10. THIS TERMINAL IS A STANDARD COAXIAL TERMINATION FIELD(CTF) GROUND PIN. IT'S GROUND IS COMMON WITH ALL GROUND TERMINALS VIA THE MULTILAYER PRINTED WIRING BOARD(MLPWB), ED4CD17-30, GROUND PLANE.

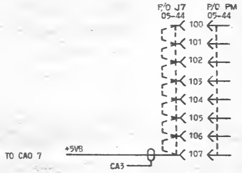
11. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....NO CAD APPARATUS INVOLVED....................................									
TO CAD 3	GRDB	CA3			GRDB	01-39 SW	B		7
TO CAD 3	+24V	CA3			+24V	01-39 SW	1C		6



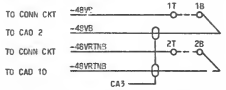
12. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
..............J7				05-44	JACK/PM	(NOTE 12)............			
	+5VB	MC		100	+5VB				
	+5VB	MC		101	+5VB				
	+5VB	MC		102	+5VB				
	+5VB	MC		103	+5VB				
	+5VB	MC		104	+5VB				
	+5VB	MC		105	+5VB				
	+5VB	MC		106	+5VB				
TO CAD 7	+5VB	CA3		107	+5VB				



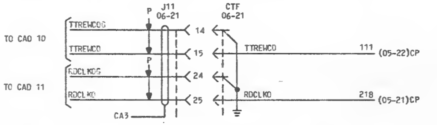
13. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....				01-40R	TS	(NOTE 13)............			
TO CAD 2	-48VB	CA3		1B	-48VB				6
TO CONN CKT	-48VB			1T	-48VB				
	-48VRTNB	MC		2B	-48VRTNB				
TO CAO 10	-48VRTNB	CA3		2T	-48VRTNB				3
TO CONN CKT	-48VRTNB			2T	-48VRTNB				



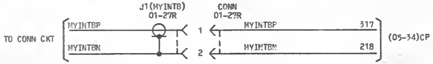
14. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
..............J11				06-21	JACK/CTF	(NOTE 14)............			
TO CAD 10	TTREWCDG	CA3	P1	14	TTREWCDG				10
TO CAD 10	TTREWCD	CA3	P1	15	TTREWCD	05-22 CP	111		
TO CAD 11	RDCLKDG	CA3	P2	24	RDCLKDG				10
TO CAD 11	RDCLKD	CA3	P2	25	RDCLKD	05-21 CP	218		



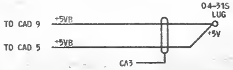
15. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
.... J1(MYINTB)				01-27R	CONNECTOR	(NOTE 15)............			
TO CONN CKT	MYINTBP		CX1	1	MYINTBP	05-34 CP	317		202
TO CONN CKT	MYINTBN		CX1	2	MYINTBN	05-34 CP	218		202



16. THE FOLLOWING SHOWS THE SYMBOLIC EQUIVALENT OF THE TABULAR REPRESENTATION:

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	WIRE METHOD	SYM	TERMINAL	LEAD DESIG	TO TERMINATION	TERMINAL	OPT	NOTE
....				04-31S	LUG	(NOTE 16)................			
TO CAD 9	+5VB	CA3		+5V	+5VB				4
TO CAD 5	+5VB	CA3		+5V	+5VB				2



TAPE DATA CONTROLLER
②
DWG SIZE 6S
ISSUE 5AC
BELL LABORATORIES
SD-1C904-01
G81

CAD 1

UNIT SYMBOL

ELEMENT IDENTIFIER

A

TDC SP1

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
MYINTAN	O	02-27R-2	05-34-219	1/1	202
MYINTAP	O	02-27R-1	05-34-318	1/1	202
MYINTBN	O	01-27R-2	05-34-218	1/1	202
MYINTBP	O	01-27R-1	05-34-317	1/1	202
MYRAN	I	02-28R-2	05-33-311	1/2	202
MYRAP	I	02-28R-1	05-33-213	1/2	202
MYRBN	I	01-28R-2	05-33-208	1/2	202
MYRBP	I	01-28R-1	05-33-308	1/2	202
MYSAN	O	02-30R-2	05-33-118	1/2	202
MYSAP	O	02-30R-1	05-33-218	1/2	202
MYSBN	O	01-30R-2	05-33-219	1/2	202
MYSBP	O	01-30R-1	05-33-318	1/2	202

ELEMENT IDENTIFIER

B

TDC PWR

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
+24V	P	05-44-112	05-39-112	6/1	
+24V	P	05-44-012	05-39-112	6/1	
-48VA	P	05-44-019	05-44-019	6/2	
-48VAB	P	05-44-018	05-44-018	6/2	
-48VAC	P	05-44-017	05-44-017	6/2	
-48VAD	P	05-44-117	05-44-117	6/2	
-48VAE	P	05-44-118	05-44-118	6/2	
-48VAF	P	05-44-119	05-44-119	6/2	
-48VAG	P	05-39-119	05-39-119	6/1	
-48VAH	P	05-39-118	05-39-118	6/1	
-48VAI	P	05-39-117	05-39-117	6/1	
-48VAJ	P	05-39-017	05-39-017	6/1	
-48VAK	P	05-39-018	05-39-018	6/1	
-48VAL	P	05-39-019	05-39-019	6/1	
-48VB	I	01-40R-1T	01-40R-1T	6/4	
-48VRTNA	I	05-44-014	05-44-014	6/2	
-48VRTNB	I	01-40R-2T	01-40R-2T	6/4	
-48VRTNC	I	05-39-014	05-39-014	6/1	
-48VRTND	P	05-39-015	05-39-015	6/1	
-48VRTNE	P	05-39-016	05-39-016	6/1	
-48VRTNF	P	05-39-114	05-39-114	6/1	
-48VRTNG	P	05-39-115	05-39-115	6/1	
-48VRTNH	P	05-39-116	05-39-116	6/1	
-48VRTNI	P	05-44-015	05-44-015	6/2	
-48VRTNJ	P	05-44-016	05-44-016	6/2	
-48VRTNK	P	05-44-116	05-44-116	6/2	
-48VRTNL	P	05-44-115	05-44-115	6/2	
-48VRTNM	P	05-44-114	05-44-114	6/2	
FA	O	05-44-314	05-39-314	6/1	
FRGRD	G	01-40R-3T	01-40R-3T	6/4	
GRDB	G	05-44-319	05-44-319	6/2	
NPA	I	05-44-315	05-39-315	6/1	
PA	O	05-44-313	05-39-313	6/1	
PA	O	05-44-310	05-39-313	6/1	
PAT	I	05-44-312	05-39-312	6/1	

ELEMENT IDENTIFIER

C

SYNCHRONOUS DATA SET CONTROLLER

TERM. MODIFIER	FUNC	ACCESS TERM.	FS TERM.	LOC FS/SYM	NOTE
CTSP-CB	I	01-19-5F	05-24-218	7/2	2 207
DCDP-CF	I	01-19-8F	05-24-313	7/2	2 207
DSRP-CC	I	01-19-6F	05-24-317	7/2	2 207
DTRP-CD	O	01-19-20F	05-24-310	7/2	2 207
FG-AA	G	01-19-1F	01-40R-3T	6/4	2 207
RCP-DD	I	01-19-17F	05-24-213	7/2	2 207
RDN-BB	I	01-19-3F	05-24-214	7/2	2 207
RNGP-CE	I	01-19-22F	05-24-314	7/2	2 207
RTSP-CA	O	01-19-4F	05-24-106	7/2	2 207
SG-AB	G	01-19-7F	05-24-210	7/2	2 207
TCP-DB	I	01-19-15F	05-24-318	7/2	2 207
TRDN-BA	O	01-19-2F	05-24-105	7/2	2 207

TAPE DATA CONTROLLER	DWG SIZE C2	ISSUE 5AC
BELL LABORATORIES	SD-1C904-01	GB2

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CAD 2

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	NO CAD APPARATUS INVOLVED	....							
TO CAD 4	+24VS	CA3			+24VS	01-39 SW	1NO		7
TO CAD 9	-48VBS	CA3			-48VBS	01-39 SW	5NO		5
TO CAD 15	PN48	CA3			PN48	01-39 SW	3NO		7
TO CAD 3	+24VS	CA3			+24VS	01-39 SW	1NO		7
TO CAD 9	+24VS	CA3			+24VS	01-39 SW	1NO		6
|	-48VB	CA3			-48VB	01-39 SW	5C		5
TO CAD 3	-48VA	CA3			-48VA	01-39 SW	3C		7
|	+24V	CA3			+24V	01-39 SW	1C		6
|	GRDB	CA3			GRDB	01-39 SW	B		7

CAD 3

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	NO CAD APPARATUS INVOLVED	....							
TO CAD 2	GRDB	CA3			GRDB	05-44 PM	319		7
|	+24V	CA3			+24V	05-44 PM	112		6
|	-48VA	CA3			-48VA	05-44 PM	019		7
|	+24V	CA3			+24V	05-44 PM	012		6
|	+24VS	CA3			+24VS	05-44 PM	011		7

CAD 4

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	NO CAD APPARATUS INVOLVED	....							
TO CAD 2	+24VS	CA3			+24VS	05-39 PM	011		7

CAD 5

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J7			05-44	JACK/PM	(NOTE 12)................			
	+5VB	MC		001	+5VB				
	+5VB	MC		002	+5VB				
	+5VB	MC		003	+5VB				
	+5VB	MC		004	+5VB				
	+5VB	MC		005	+5VB				
	+5VB	MC		006	+5VB				
	+5VB	MC		007	+5VB				
	+5VB	MC		100	+5VB				
	+5VB	MC		101	+5VB				
	+5VB	MC		102	+5VB				
	+5VB	MC		103	+5VB				
	+5VB	MC		104	+5VB				
	+5VB	MC		105	+5VB				
	+5VB	MC		106	+5VB				
TO CAD 7	+5VB	CA3		107	+5VB				2

CAD 6

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J8			05-39	JACK/PM	(NOTE 12)................			
	+5VA	MC		001	+5VA				
	+5VA	MC		002	+5VA				
	+5VA	MC		003	+5VA				
	+5VA	MC		004	+5VA				
	+5VA	MC		005	+5VA				
	+5VA	MC		006	+5VA				
	+5VA	MC		007	+5VA				
	+5VA	MC		100	+5VA				
	+5VA	MC		101	+5VA				
	+5VA	MC		102	+5VA				
	+5VA	MC		103	+5VA				
	+5VA	MC		104	+5VA				
	+5VA	MC		105	+5VA				
	+5VA	MC		106	+5VA				
TO CAD 8	+5VA	CA3		107	+5VA				2

CAD 7

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....				04-31S	LUG	(NOTE 16)................			
TO CAD 9	+5VB	CA3		+5V	+5VB				4
TO CAD 5	+5VB	CA3		+5V	+5VB				2
....				04-32S	LUG	(NOTE 16)................			
TO CAD 9	GRDB	CA3		GRD	GRDB				4
TO CAD 17	GRDB	CA3		GRD	GRDB				2

CAD 8

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....				04-16S	LUG	(NOTE 16)................			
TO CAD 6	+5VA	CA3		+5V	+5VA				2
....				04-17S	LUG	(NOTE 16)................			
TO CAD 9	GRDA	CA3		GRD	GRDA				3
TO CAD 18	GRDA	CA3		GRD	GRDA				2

CAD 9

POWER

—TO CONNECTION—					—FROM CONNECTION—				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....				01-40R	TS	(NOTE 13)................			
TO CAD 2	-48VB	CA3		1B	-48VB				6
TO CONN CKT	-48VB			1T	-48VB				
	-48VRTNB	MC		2B	-48VRTNB				
TO CAD 10	-48VRTNB	CA3		2T	-48VRTNB				3
TO CONN CKT	-48VRTNB			2T	-48VRTNB				
TO CAD 8	GRDA	CA3		3B	GRDA				3
TO CAD 7	GRDB	CA3		3B	GRDB				3
	FRGRD	MC		3B	FRGRD				
TO CAD 10	FRGRD	CA3		3T	FRGRD				4
TO CONN CKT	FRGRD			3T	FRGRD				
TO CAD 2	-48VBS	CA3		4B	-48VBS				5
TO CAD 10	-48VBS	CA3		4T	-48VBS				5
TO CAD 2	+24VS	CA3		5B	+24VS				6
TO CAD 10	+24VS	CA3		5T	+24VS				6
TO CAD 7	+5VB	CA3		6B	+5VB				4
TO CAD 10	+5VB	CA3		6T	+5VB				4

TAPE DATA CONTROLLER

DWG SIZE
C2

ISSUE
2A

BELL LABORATORIES
SD-1C904-01
GB3

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10/16/75

CAD 10

CTT CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J9			04-04R	JACK/CTT	(NOTE 14).................			
TO CAD 14	TTMSTPO	CA3	P1	2	TTMSTPO				
|	TTMSTPOG	CA3	P1	3	TTMSTPOG				
TO CAD 12	TTFFOG	CA3	P2	4	TTFFOG				
|	TTSFOG	CA3	P3	5	TTSFOG				
TO CAD 14	TTBOTAOG	CA3	P17	7	TTBOTAOG				
TO CAD 12	TTFROG	CA3	P4	8	TTFROG				
|	TTSROG	CA3	P5	9	TTSROG				
|	TTSELOG	CA3	P6	10	TTSELOG				
TO CAD 14	TTINITOG	CA3	P7	11	TTINITOG				
TO CAD 12	TTREWCOG	CA3	P8	12	TTREWCOG				
TO CAD 14	MANENOG	CA3	P9	13	MANENOG				
TO CAD 13	TTRDYOG	CA3	P10	14	TTRDYOG				
|	RWDINGOG	CA3	P11	15	RWDINGOG				
|	TOROG	CA3	P12	16	TOROG				
|	TIMAOG	CA3	P13	17	TIMAOG				
|	TTEOTAOG	CA3	P14	18	TTEOTAOG				
|	LPEWOG	CA3	P15	19	LPEWOG				
|	CARTWEOG	CA3	P16	20	CARTWEOG				
TO CAD 9	FRGRD	CA3		21	FRGRD				4
|	-48VRTNB	CA3		22	-48VRTNB				5
|	+5VB	CA3		24	+5VB				4
|	-48VBS	CA3		25	-48VBS				5
TO CAD 12	TTFFO	CA3	P2	26	TTFFO				
|	TTSFO	CA3	P3	27	TTSFO				
|	TTFRO	CA3	P4	28	TTFRO				
|	TTSRO	CA3	P5	29	TTSRO				
|	TTSELO	CA3	P6	30	TTSELO				
TO CAD 14	TTINITO	CA3	P7	31	TTINITO				
TO CAD 12	TTREWCO	CA3	P8	32	TTREWCO				
TO CAD 14	MANENO	CA3	P9	33	MANENO				
TO CAD 13	TTRDYO	CA3	P10	34	TTRDYO				
|	RWDINGAO	CA3	P11	36	RWDINGAO				
|	TORO	CA3	P12	38	TORO				
|	TIMAO	CA3	P13	40	TIMAO				
TO CAD 14	TTBOTAO	CA3	P17	42	TTBOTAO				
TO CAD 13	TTEOTAO	CA3	P14	44	TTEOTAO				
|	LPEWO	CA3	P15	47	LPEWO				
|	CARTWEO	CA3	P16	49	CARTWEO				
TO CAD 9	+24VS	CA3		50	+24VS				6

CAD 11

CTT CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J10			04-10R	JACK/CTT	(NOTE 14).................			
TO CAD 14	WTA00G	CA3	P1	1	WTA00G				
|	RTA00G	CA3	P2	2	RTA00G				
|	WTA10G	CA3	P3	3	WTA10G				
|	RTA10G	CA3	P4	4	RTA10G				
TO CAD 12	WRENABOG	CA3	P5	5	WRENABOG				
TO CAD 13	WRDATAG	CA3	P6	6	WRDATAG				
TO CAD 12	RDDATAOG	CA3	P7	14	RDDATAOG				
|	RDCLKOG	CA3	P8	15	RDCLKOG				
TO CAD 13	DATDETOG	CA3	P9	16	DATDETOG				
|	DATDETO	CA3	P9	18	DATDETO				
TO CAD 14	WTA00	CA3	P1	19	WTA00				
|	RTA00	CA3	P2	20	RTA00				
|	WTA10	CA3	P3	21	WTA10				
|	RTA10	CA3	P4	22	RTA10				
TO CAD 12	WRENABO	CA3	P5	23	WRENABO				
TO CAD 13	WRDATA	CA3	P6	24	WRDATA				
TO CAD 12	RDDATAO	CA3	P7	35	RDDATAO				
|	RDCLKO	CA3	P8	36	RDCLKO				

CAD 12

CTF CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J11			06-21	JACK/CTF	(NOTE 14).................			
TO CAD 10	TTREWCOG	CA3	P1	14	TTREWCOG				10
|	TTREWCO	CA3	P1	15	TTREWCO	05-22 CP	111		
TO CAD 11	RDCLKOG	CA3	P2	24	RDCLKOG				10
|	RDCLKO	CA3	P2	25	RDCLKO	05-21 CP	218		
|	RDDATAOG	CA3	P3	34	RDDATAOG				10
|	RDDATAO	CA3	P3	35	RDDATAO	05-21 CP	318		
	............J11			06-22	JACK/CTF	(NOTE 14).................			
TO CAD 10	TTSELOG	CA3	P4	04	TTSELOG				10
|	TTSELO	CA3	P4	05	TTSELO	05-22 CP	315		
|	TTSFOG	CA3	P5	14	TTSFOG				10
|	TTSFO	CA3	P5	15	TTSFO	05-22 CP	116		
|	TTFROG	CA3	P6	24	TTFROG				10
|	TTFRO	CA3	P6	25	TTFRO	05-22 CP	016		
|	TTFFOG	CA3	P7	34	TTFFOG				10
|	TTFFO	CA3	P7	35	TTFFO	05-22 CP	216		
	............J11			06-23	JACK/CTF	(NOTE 14).................			
TO CAD 10	TTSROG	CA3	P8	04	TTSROG				10
|	TTSRO	CA3	P8	05	TTSRO	05-22 CP	316		
TO CAD 11	WRENABOG	CA3	P9	14	WRENABOG				10
|	WRENABO	CA3	P9	15	WRENABO	05-22 CP	100		

CAD 13

CTF CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J12			06-18	JACK/CTF	(NOTE 14).................			
TO CAD 10	CARTWEOG	CA3	P1	34	CARTWEOG				10
|	CARTWEO	CA3	P1	35	CARTWEO	05-19 CP	201		
	............J12			06-19	JACK/CTF	(NOTE 14).................			
TO CAD 10	TIMAOG	CA3	P2	04	TIMAOG				10
|	TIMAO	CA3	P2	05	TIMAO	05-19 CP	118		
|	TOROG	CA3	P3	14	TOROG				10
|	TORO	CA3	P3	15	TORO	05-19 CP	018		
|	RWDINGOG	CA3	P4	24	RWDINGOG				10
|	RWDINGAO	CA3	P4	25	RWDINGAO	05-19 CP	019		
|	TTRDYOG	CA3	P5	34	TTRDYOG				10
|	TTRDYO	CA3	P5	35	TTRDYO	05-19 CP	301		
	............J12			06-20	JACK/CTF	(NOTE 14).................			
TO CAD 10	LPEWOG	CA3	P6	04	LPEWOG				10
|	LPEWO	CA3	P6	05	LPEWO	05-19 CP	300		
|	TTEOTAOG	CA3	P7	14	TTEOTAOG				10
|	TTEOTAO	CA3	P7	15	TTEOTAO	05-20 CP	113		
TO CAD 11	DATDETOG	CA3	P8	24	DATDETOG				10
|	DATDETO	CA3	P8	25	DATDETO	05-19 CP	219		
|	WRDATAG	CA3	P9	34	WRDATAG				10
|	WRDATA	CA3	P9	35	WRDATA	05-20 CP	312		

CAD 14

CTF CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J13			06-18	JACK/CTF	(NOTE 14).................			
TO CAD 10	TTINITOG	CA3	P1	26	TTINITOG				10
|	TTINITO	CA3	P1	27	TTINITO	05-22 CP	209		
|	TTMSTPOG	CA3	P2	36	TTMSTPOG				10
|	TTMSTPO	CA3	P2	37	TTMSTPO	05-22 CP	309		
	............J13			06-19	JACK/CTF	(NOTE 14).................			
TO CAD 10	TTBOTAOG	CA3	P8	26	TTBOTAOG				10
|	TTBOTAO	CA3	P8	27	TTBOTAO	05-20 CP	302		
|	MANENOG	CA3	P3	36	MANENOG				10
|	MANENO	CA3	P3	37	MANENO	05-19 CP	009		
	............J13			06-20	JACK/CTF	(NOTE 14).................			
TO CAD 11	WTA00G	CA3	P4	06	WTA00G				10
|	WTA00	CA3	P4	07	WTA00	05-22 CP	218		
|	WTA10G	CA3	P5	16	WTA10G				10
|	WTA10	CA3	P5	17	WTA10	05-22 CP	017		
|	RTA00G	CA3	P6	26	RTA00G				10
|	RTA00	CA3	P6	27	RTA00	05-22 CP	117		
|	RTA10G	CA3	P7	36	RTA10G				10
|	RTA10	CA3	P7	37	RTA10	05-22 CP	317		

CAD 15

POWER

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	......................NO CAD APPARATUS INVOLVED......................								
TO CAD 2	PN48	CA3			PN48	05-28 CP	317		7

CAD 16

SPI CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
	............J1(MYINTB)			01-27R	CONNECTOR	(NOTE 15).................			
TO CONN CKT	MYINTBP		CX1	1	MYINTBP	05-34 CP	317		202
|	MYINTBN		CX1	2	MYINTBN	05-34 CP	218		202
	............J2(MYRB)			01-28R	CONNECTOR	(NOTE 15).................			
TO CONN CKT	MYRBP		CX2	1	MYRBP	05-33 CP	308		202
|	MYRBN		CX2	2	MYRBN	05-33 CP	208		202

TAPE DATA CONTROLLER

DWG SIZE C2

ISSUE 2A

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CAD 16

(CONT'D)

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	J3(MYSB)			01-30R	CONNECTOR	(NOTE 15)................			
TO CONN CKT	MYSBP		CX3	1	MYSBP	05-33 CP	318		202
|	MYSBN		CX3	2	MYSBN	05-33 CP	219		202
....	J4(MYINTA)			02-27R	CONNECTOR	(NOTE 15)................			
TO CONN CKT	MYINTAP		CX4	1	MYINTAP	05-34 CP	318		202
|	MYINTAN		CX4	2	MYINTAN	05-34 CP	219		202
....	J5(MYRA)			02-28R	CONNECTOR	(NOTE 15)................			
TO CONN CKT	MYRAP		CX5	1	MYRAP	05-33 CP	213		202
|	MYRAN		CX5	2	MYRAN	05-33 CP	311		202
....	J6(MYSA)			02-30R	CONNECTOR	(NOTE 15)................			
TO CONN CKT	MYSAP		CX6	1	MYSAP	05-33 CP	218		202
|	MYSAN		CX6	2	MYSAN	05-33 CP	118		202

CAD 17

POWER

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	J14			05-44	JACK/PM	(NOTE 12)................			
	GRDB	MC		201	GRDB				
	GRDB	MC		202	GRDB				
	GRDB	MC		203	GRDB				
	GRDB	MC		204	GRDB				
	GRDB	MC		205	GRDB				
	GRDB	MC		206	GRDB				
	GRDB	MC		207	GRDB				
	GRDB	MC		300	GRDB				
	GRDB	MC		301	GRDB				
	GRDB	MC		302	GRDB				
	GRDB	MC		303	GRDB				
	GRDB	MC		304	GRDB				
	GRDB	MC		305	GRDB				
	GRDB	MC		306	GRDB				
TO CAD 7	GRDB	CA3		307	GRDB				2

CAD 18

POWER

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	J15			05-39	JACK/PM	(NOTE 12)................			
	GRDA	MC		201	GRDA				
	GRDA	MC		202	GRDA				
	GRDA	MC		203	GRDA				
	GRDA	MC		204	GRDA				
	GRDA	MC		205	GRDA				
	GRDA	MC		206	GRDA				
	GRDA	MC		207	GRDA				
	GRDA	MC		300	GRDA				
	GRDA	MC		301	GRDA				
	GRDA	MC		302	GRDA				
	GRDA	MC		303	GRDA				
	GRDA	MC		304	GRDA				
	GRDA	MC		305	GRDA				
	GRDA	MC		306	GRDA				
TO CAD 8	GRDA	CA3		307	GRDA				2

CAD 19

SDSC CONNECTIONS

TO CONNECTION					FROM CONNECTION				
DESTINATION	LEAD DESIG	METHOD	WIRE SYM	TERMINAL	LEAD DESIG	TERMINATION	TERMINAL	OPT	NOTE
....	J16			01-19	CONNECTOR	(NOTE 15)................			
TO CONN CKT	FG-AA			1F	FG-AA	01-40R TS	3T	Z	207
|	TRDN-BA			2F	TRDN-BA	05-24 CP	105	Z	207
|	RDN-BB			3F	RDN-BB	05-24 CP	214	Z	207
|	RTSP-CA			4F	RTSP-CA	05-24 CP	106	Z	207
|	CTSP-CB			5F	CTSP-CB	05-24 CP	218	Z	207
|	DSRP-CC			6F	DSRP-CC	05-24 CP	317	Z	207
|	SG-AB			7F	SG-AB	05-24 CP	210	Z	207
|	DCDP-CF			8F	DCDP-CF	05-24 CP	313	Z	207
|	TCP-DB			15F	TCP-DB	05-24 CP	318	Z	207
|	RCP-DD			17F	RCP-DD	05-24 CP	213	Z	207
|	DTRP-CD			20F	DTRP-CD	05-24 CP	310	Z	207
|	RNGP-CE			22F	RNGP-CE	05-24 CP	314	Z	207

TAPE DATA CONTROLLER

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